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AP 2426

EMC Design Guideline for Microcontroller Board Layout

Microcontrollers

Infineon technologies

Never stop thinking.

EMC Design Guideline

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Previous Version:	04.99	
Page	Subjects (major changes since last revision)	
6	New chapter about EMC basics implemented	
4 - 31	General update	

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1 How to use this Guideline

The topic of electromagnetic compatibility is important for the functionality and security of electronic devices. Today's designers have to deal with permanently increasing system frequencies, changing power limits, high density layouts by more complex systems and the steady need of low manufacturing cost. Therefore it is necessary to look after EMC.

In this EMC design guideline we are concentrating on some rules and examples for PCB layout. By using these rules, it is possible to prevent high electromagnetic emission already through a good PCB design. This design guide is made for various applications with their different purpose. Therefore, each application will show varying strong reaction on the realised EMC design improvements.

The rules are faced mainly to the problem of electromagnetic emission (EME). Due to the fact that an EME optimised board layout is not so sensitive to interference, using these rules will also decrease the susceptibility (EMS).

This guideline is structured in order to fit the needs of a PCB designer. Basics, board stack and trace design are followed by various rules for decoupling and 'further hints'.

2 About EMC

Electromagnetic disturbance is the interference to the normal function of an electric circuit, by coupling in an additional voltage. There are various paths to couple into a circuit and various ways to avoid these interferences.

It has to be seen, that measures to realise a good EMC-behaviour of an application have to be started and implemented already into the first steps of development. Measures and actions taken later on, at an already manufactured printed-circuit board (PCB), are not as effective and aditionally will lead to higher costs.

The EM disturbance needs three steps:

The source: This is the place where the noise or disturbance is created. Reason for this can be e.g. fast signals, fast rise time, resonance, antenna structures, wrong termination, reflections and electric potential differences. (Goal: EM-suppression at the 'source')

The victim: The electrical circuit which becomes influenced by the disturbance coming from the 'source'. This disturbance can lead to some imperceptible noise added on a signal. But this disturbance can also have some major impact on the functionality of a signal or the whole application. (Goal: Low susceptibility to emission at the 'victim')

The coupling path: (*See figure (2)*) The path or medium where the disturbance is distributed from the 'source' to the 'victim'. (Goal: the 'coupling path' has to be made inefficient).

At all three steps it is possible to damp or even eliminate the electromagnetic disturbance by various measures.

Interference current and voltage of an electrical system can be described as common-mode (CM) or differential-mode (DM).

Figure 1

Common-mode *interference is an asymmetrical disturbance. It often occurs between a cable system and their electrical reference potential.*

Signal and noise current have the same (a common) direction in the loop.

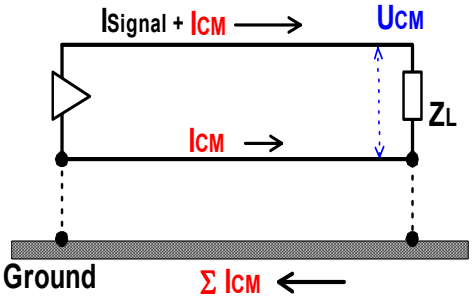

Figure 1a

Differential-mode *interference is a symmetrical disturbance, which occurs between two traces or lines. One of these lines can also be the ground path.*

Signal and noise current have a different direction in the electrical loop.

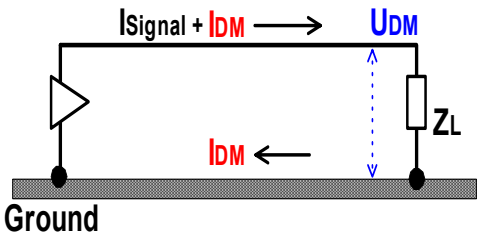

Figure 1b

The layout structure of a printed-circuit board (PCB) is essential for the common mode (CM) emission and has to be designed very carefully.

There are four paths for transmitting electromagnetic disturbance:

Figure 2

Coupling by electromagnetic radiation:
A trace or any metal layout structure is effective as victim-antenna at the length of L > λ/4

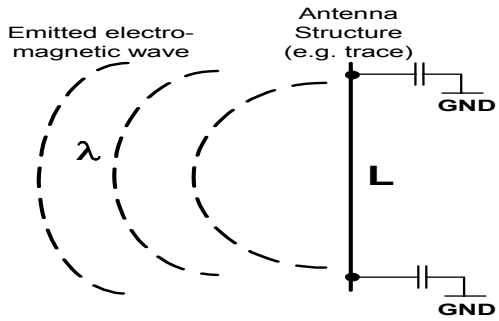

Figure 2a

Electric / Capacitive coupling:
Coupling between two traces with different electrical potential. Because of this potential difference, an electric field is caused and disturbances are influencing the victim line.
With U_D is the incoupled voltage.

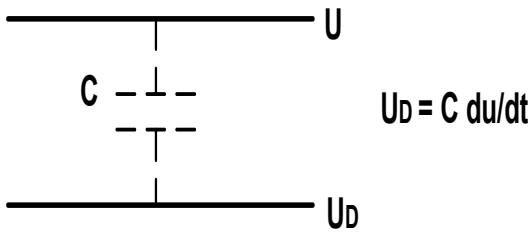

Figure 2b

Magnetic / Inductive coupling:
Coupling between two or more current-carrying conductors. The magnetic flux, connected to the current is interspersing the opposite circuit (victim line) with parasitic voltage

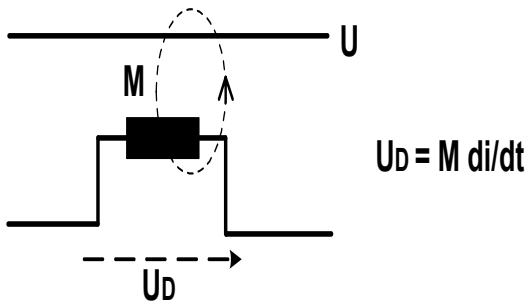

Figure 2c

Galvanic coupling:
happens if a common impedance is used from two or more electric circuits. This can be a ground system which works as a common back-current path for several signals.

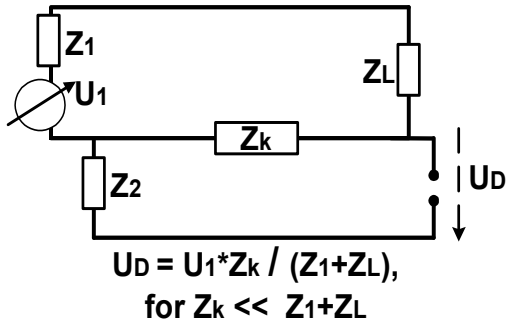

Figure 2d

3 Board and Trace Design

In the first step, the power supply system should be designed (power bus design). A proper power bus design is the basic requirement for voltage stability and reduced electromagnetic emission.

Separate digital and analogue supply system.

Decide for PCB Technology: two layers, four or more layers.

Note: Concerning EMC, a good design of two layer boards is more difficult to realise than four or more layer boards.

3.1 Two Layers

Keep power and ground nets (which belong to each other) close together in order to reduce impedance.

The GND trace should be as close to the V_{DD} trace as possible. Best choice is to design them in parallel. If the current and the belonging ground trace have to go different ways, there will be different potentials and common mode problems.

(The picture shows GND-trace and V_{DD}-trace on different sides of the PCB)

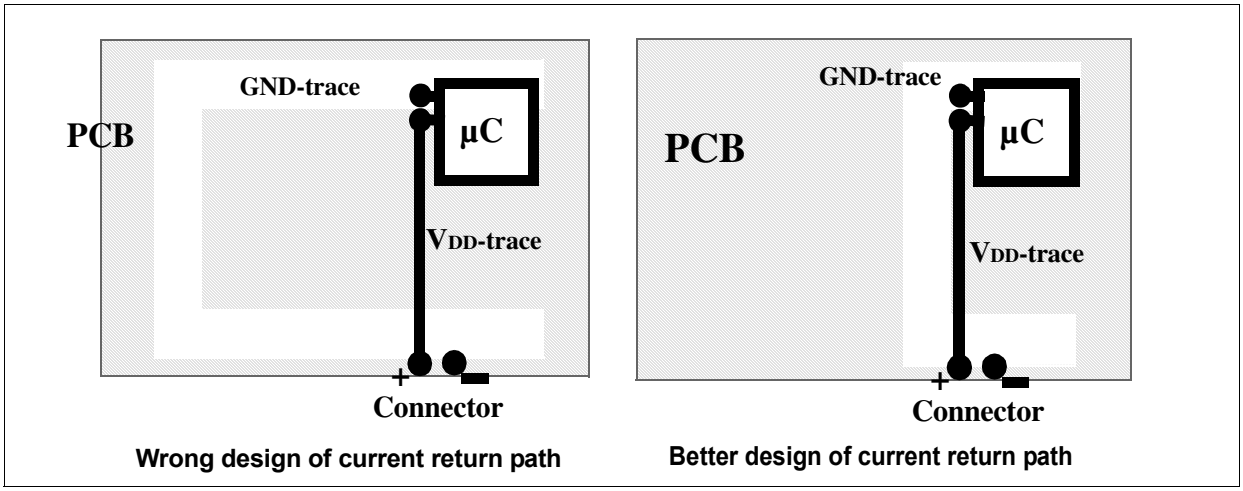

Figure 3 Design of Ground Traces

In general, power and ground traces should lead directly from the supply connector to each component / functional unit. If possible use one side as a complete ground plane for an optimised current flow.

Ground area fills have to be handled with care. Otherwise emission may increase, because of resonance structures and antenna effects. Connect them by several vias or wide traces together with the reference ground of the board. Because there are various effects which influence the radiation and susceptibility of the PCB, each application has to be handled in special.

3.2 Multilayer Board:

3.2.1 Board Stack

Design at least one power/ground sandwich: Realise power and ground planes on adjacent layers.

The smaller the distance between power and ground layer, the lower the impedance of the power supply becomes. This is the basic requirement for the voltage supply stability (see Figure 2).

Use the shielding effects of supply planes to reduce electromagnetic emission: If you have more than four layers you may design a signal layer for critical traces between two continuos layers. That provides a good back current path, which is not interfering with other signals. As well, it is effective as a shield against radiation to the outside of the PCB. If there is enough space, implement more extra ground planes in your layer stack, so that each signal layer has its own corresponding ground layer. To have an extra ground plane for a signal layer makes it possible to keep the determined characteristic wave impedance.

Suggested Layer Stacks:

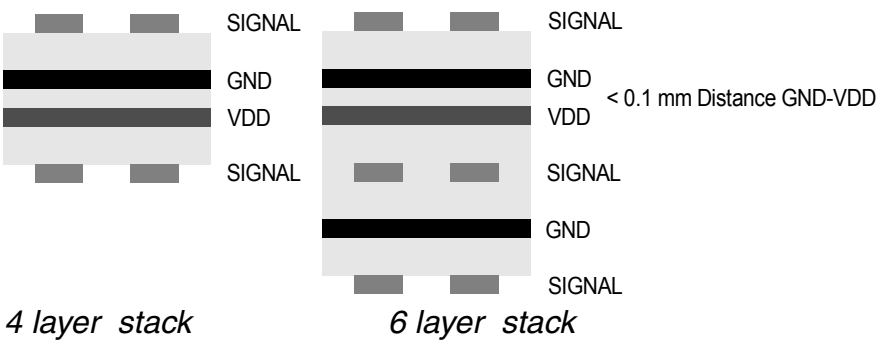

Figure 4 Multilayer Stack Proposal

3.2.2 Board Layout

Signal currents use both power plane and ground plane as return path. Keep supply planes as “clean” as possible: Avoid areas of high impedance (groups of vias, gaps). Avoid segments in the ground planes. This measure keeps the current return path short.

Example for placements of vias are shown in figure 5. In the upper-left case the return current is forced to flow around the group of vias. In the upper-right case the current can flow nearly directly from one side to the other. The best solution for a current return path is shown in the lower-left configuration.

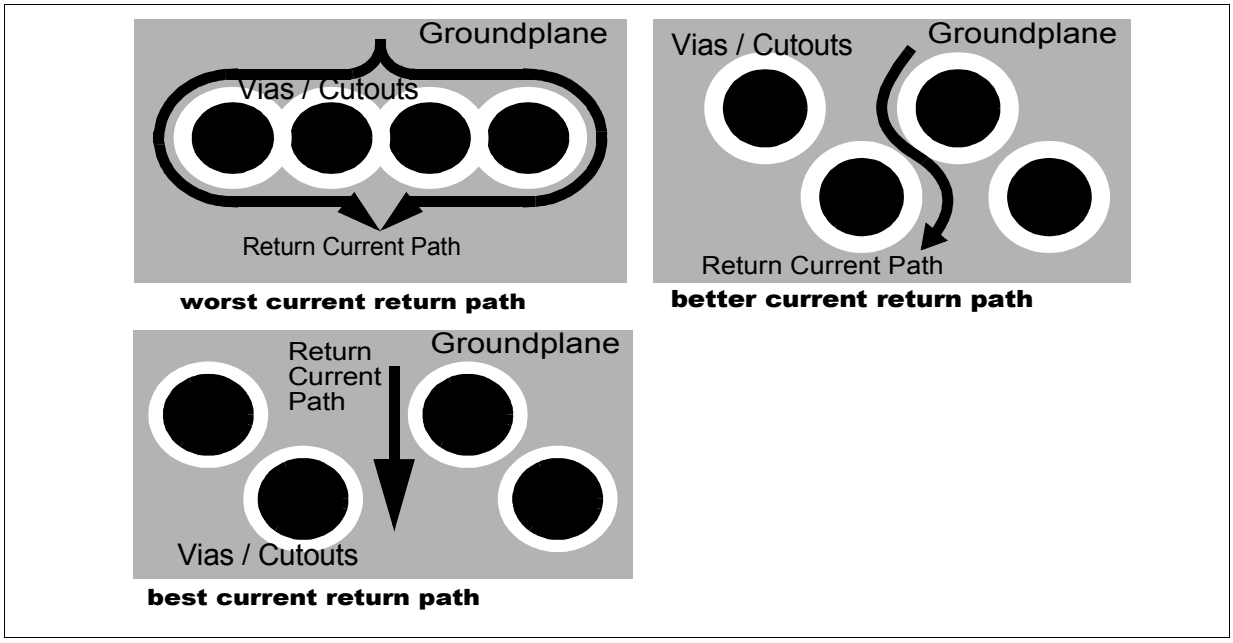

Figure 5 No Blocking of Current Return Path

For DC-Voltage the current return path takes the way of lowest impedance, but in the area of high-frequency the current return path follows the path of least inductance (see figure 6).

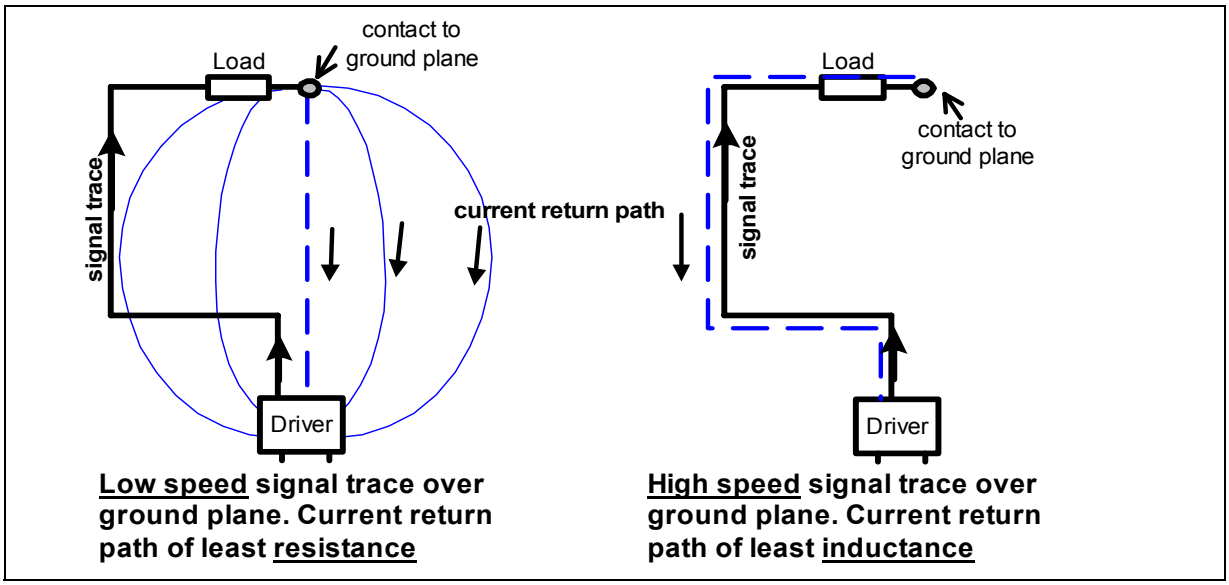

Figure 6 Return Current of High Speed Signals

3.2.3 Splitted Planes

In some cases, splitting power or ground planes can bring a big improvement to the EMC behaviour and for signal integrity. This splitting has to be done under several considerations of the signal and current flow. A separation of very sensitive parts from noisy areas of a PCB keeps the disturbance low and minimises the possibility of galvanic coupling.

If the V_{DD} plane is to be divided into segments, provide one area for every functional unit. These zones (if they have the same supply) should be still connected together. That influences the way and the impedance of the current flow. For the ground plane a path with low impedance has to be guaranteed

The separated zones should be connected together again at a common supply star-point, which should be close to the power supply connector or voltage regulator on the PCB.

If possible, do not design any signal traces across the separation areas. Especially, avoid high speed nets leading from one zone over to the other one !

A functional unit can contain all HF-components, all analogue components, etc. Another way of building functional units is to distinguish by supply voltage (5.0 V, 2.5 V, etc.)

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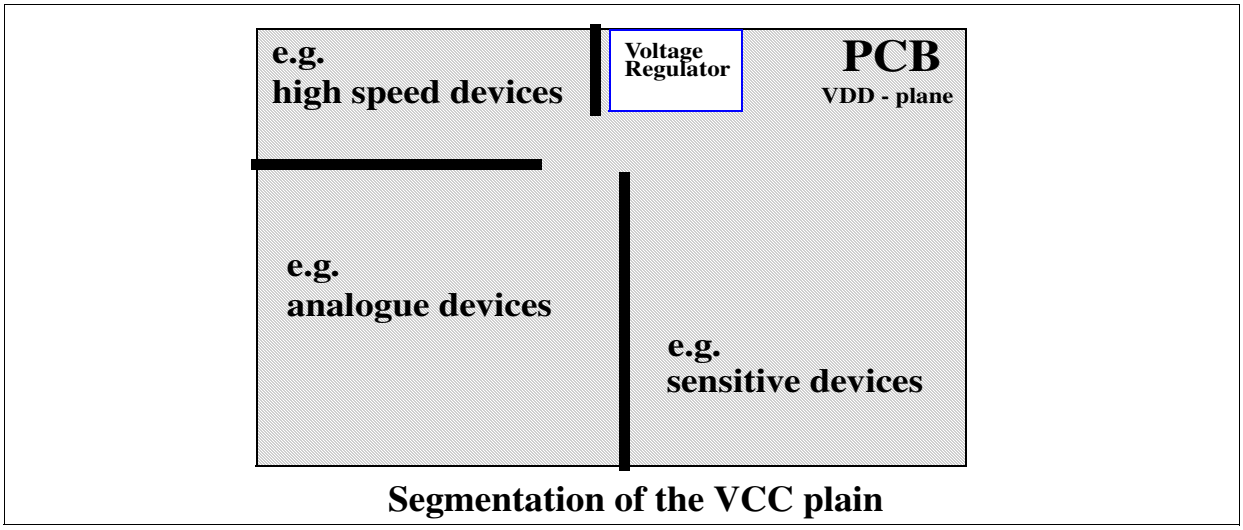

Figure 7 Example: Segmentation of the Supply Plane with Voltage Regulator as Common 'Supply Star-Point'.

3.2.4 Board Resonance

Resonances of the board structures influence the EMC behaviour in a direct way. These resonance frequencies can be seen on the emission spectra and can be critical for signal integrity. Therefore some measures have to be implemented in a PCB, to avoid resonance structures due to the board layout.

Since board resonance is mainly caused between two planes, one option is, to realise the V_{DD} power by traces. Also for designing these V_{DD} traces, the considerations from paragraph 3.2.1 to 3.2.3 should be implemented (i.e. power-star point, separate traces for different board sections, distance to ground plane).

Traces have a higher impedance compared to a plane structure. Using V_{DD} traces, local disturbances on the PCB can be prevented from spreading over the whole board. To provide the necessary current potential for switching operations, locally decoupled 'power islands' should be realised directly underneath the microcontroller and logic devices. From these islands the noise has a path of high impedance to an other device and will be kept locally.

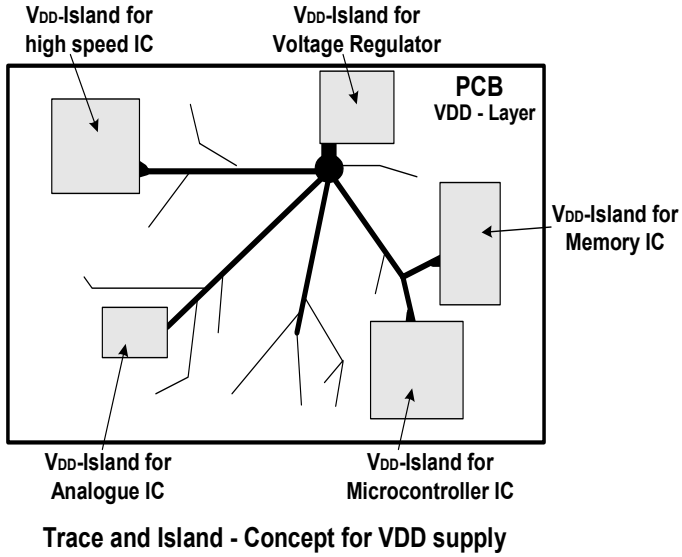

Figure 8 Example: Using V_{DD} Islands and Traces over Ground Plane.

3.3 Determine your critical nets by the following criteria.

Determine critical nets by their rise and fall times. The shorter the rise and fall times become the more high frequency components are contained in the spectrum.

This figure shows the spectra of signals with different rise times (worst case setting)

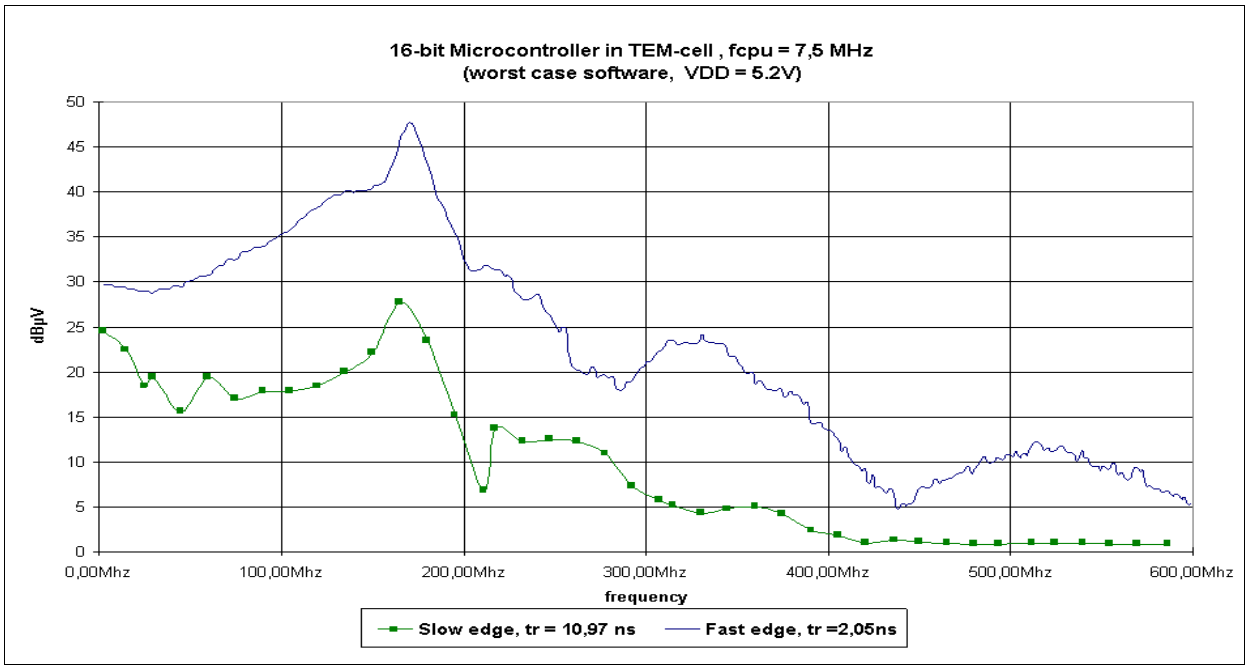

Figure 9 Effect of Rise Time on the Spectrum

Determine critical nets by driver strength.

Determine critical nets by frequency. The higher the signal frequency becomes, the higher the corresponding harmonic frequencies are.

Typical critical nets (if available):
Most critical at single chip applications:
Clock out, ALE (if no disable bit available), Data bus, Address bus, SSC (Synchronous Serial Channel)
Most critical at other applications:
Clock out, ALE, Read, Data bus, Address bus, SSC (Synchronous Serial Channel)

3.4 Set up Specific Design Rules for Your High Speed Nets.

The following design hints are only valid for simple design situations. For more complex structures it is not possible to determine general design rules. These structures have to be handled by SPICE simulation (in conjunction with 2D- or 3D-Field Solver) for establishing design rules.

To ensure Signal Integrity (SI): Take care of characteristic wave impedance of traces when using more than one layer. Determine widths of traces to guarantee the same characteristic wave impedance over the whole trace.

This figure shows the changes in characteristic wave impedance due to a smaller distance trace to groundplane or due to a wider trace. Formulas for the calculation of the characteristic wave impedance are listed in the 'Formula Appendix ' of this document.

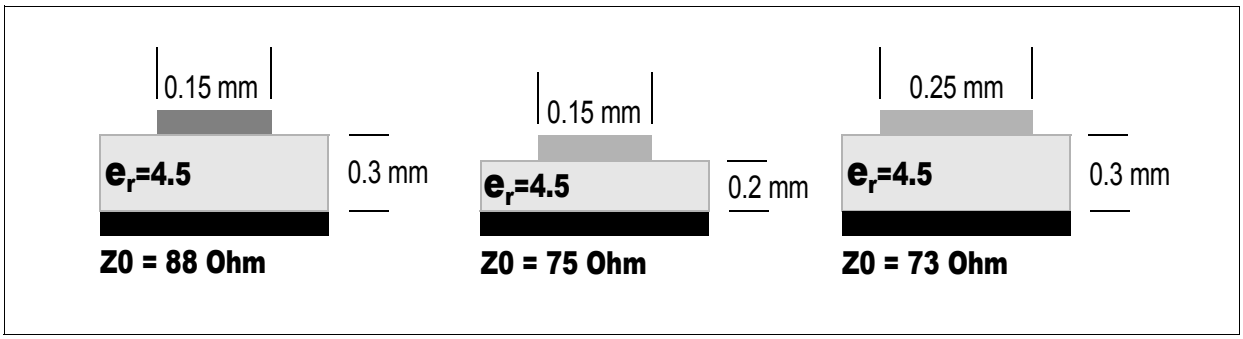

Figure 10 Wave Impedance

It should be avoided to put traces with high speed signals along edges of a PCB. Disturbances can be coupled easily into a metal casing/shielding of the application.

To ensure SI and reduce electromagnetic emission (EME): Provide series resistors close to the drivers. Optimise their values by simulation or by approximate calculation from VI-table of the driver and the trace's impedance.

There are three goals for optimisation: minimising reflection, voltage swing and emission.
To minimise reflection match the driver's Ri to Z0 by a series resistor Rx close to the driver. A matching termination of a high speed signal trace on both sides is very important, especially when the rise time of the driver signal is short in comparison to the signal propagation delay.
For optimising the voltage swing determine a series resistor Rx, that cuts half of the voltage swing on a two-point-net (with a characteristic wave impedance Z0) while regarding the non-linear Ri.

For minimising electromagnetic emission, provide resistors (20-200 Ohms) and adjust for a smooth rising edge. If provided in the microcontroller, use software settings for edge control.

To limit crosstalk (XTK): Determine a maximum overshoot on XTK. Determine a minimum distance / maximum parallel length between high speed nets in order to limit a minimum crosstalk (use simulation).

3.5 Make the placement for your PCB

Define functional units.
Classify also by speed: Analogue sensor, digital low speed, digital high speed, power elements.
Keep elements of one functional unit in close distance to keep critical signal traces as short as possible.

Provide enough space for decoupling capacitors close to the IC and spread over the whole PCB.

Provide space for series resistors within high speed traces close to the driver. But take care that the signal timing will still meet the specification.

Place oscillators adjacent to the clock driver. If an asymmetrical board stack design is used, place the crystal oscillator on the side of the PCB which has the largest distance from the reference ground layer. This can prevent a direct coupling from the crystal oscillator package into the ground system of the PCB.

For two layer boards: Keep a “distance” between functional units either by geometry or by ground trace.

3.6 Layout Your High Speed Nets

Design short traces.

Keep the return current path as short as possible at the high speed trace. In 4 or more layer boards avoid gaps or batteries of vias within a groundplane in order to keep the loop of the current return path small. On two layer boards provide power and ground nets close to the high speed trace.

The smaller the return current loop the lower the electromagnetic emission. Keep in mind that return currents can also use the V_{DD} *system!*

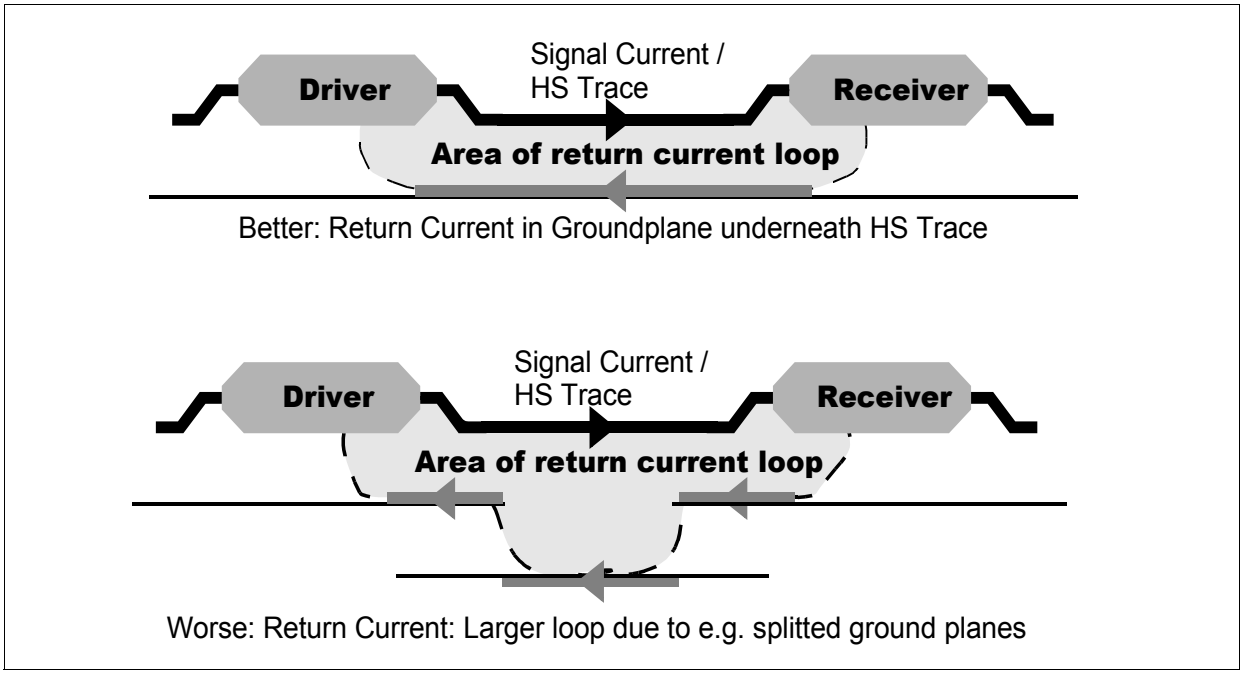

Figure 11 Return Current Loop Area for Multilayer Boards

If fast signals will be provided on the PCB, design a ground ring around each layer of your board. This ground ring should be connected by several vias on the edge of the board together to the reference ground plane. The distance from one via to the next should be not wider than 0,5cm. This builds a reference ground ring around the board, which helps to decrease radiation from the inner layer. Additionally it avoids that current at the edges of the PCB can build antenna structures and radiate to the outside.

If very high frequencies will be transferred, the distance between the connecting vias has to be even smaller. The efficiency of this measure is increasing if you have more ground planes. Then the built construction describes a faraday cage for the middle signal layers.

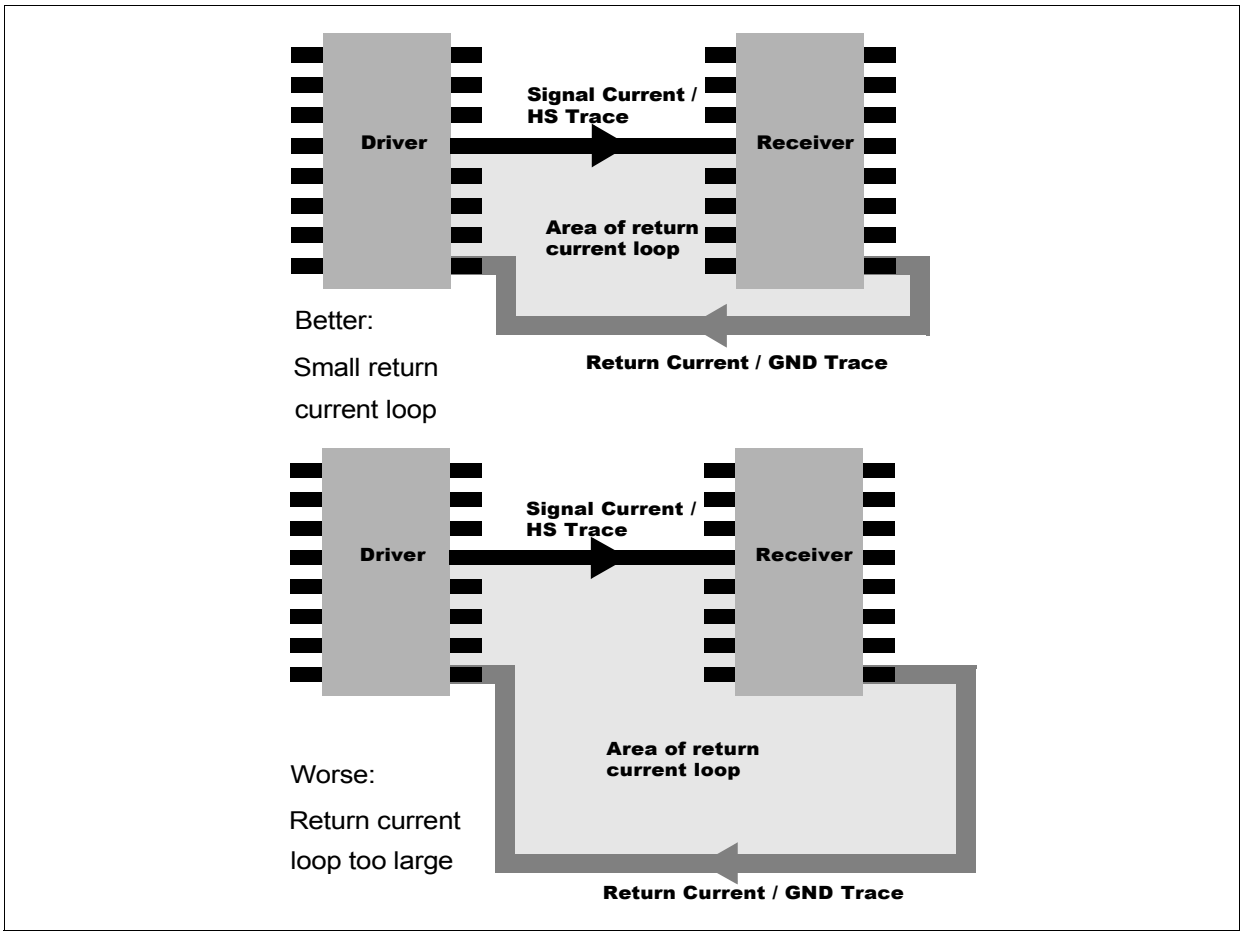

Figure 12 Return Current Loop Area for Two-Layer Boards

Avoid vias in high speed traces. Vias have an additional inductance (~500 pH normal via). Avoid turns in high speed traces. Turns mean a change in the characteristic wave impedance of a trace. Better use 45 degree turns (or even less!) than 90 degree turns. *90 degree turns mean a change in the trace's width. Changes in the trace's width cause changes in the characteristic wave impedance which will end in unwanted reflections.*

Provide room for a series resistor close to the driving component. If you have not set up a specific design rule yet, optimise the resistor value.

If you have two adjacent signal layers realise x-y-tracing to reduce crosstalk.

Place and layout decoupling capacitors.

Note: Finally design all other traces. This chapter should be kept in mind there as well.

4 Decoupling and Bypass Capacitors

4.1 Capacitors in HF-Applications

Parasitics of a capacitor

This figure shows the equivalent HF circuit of a capacitor: Besides the pure capacitance there is an Equivalent Series Inductance ESL and an Equivalent Series Resistance ESR.

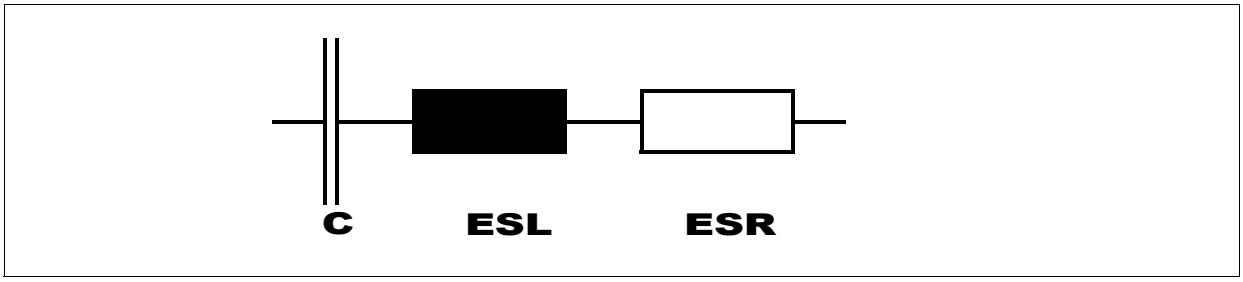

Figure 13 Equivalent Circuit of Capacitor

Impedance of a capacitor

A capacitor shows capacitive behaviour in the lower frequency range; for frequencies higher than the series resonant frequency the behaviour becomes inductive. Optimum decoupling effect is found at series resonant frequency. This information should be available in capacitor data sheets.

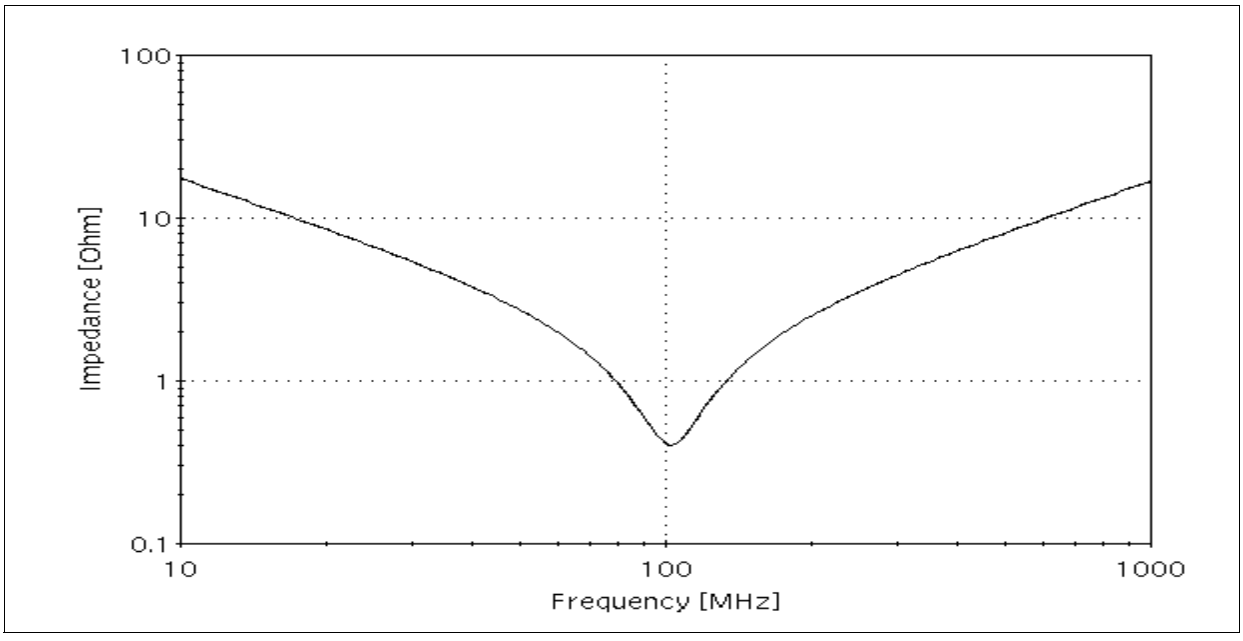

Figure 14 Impedance Characteristics of a Capacitor

4.2 Layout of Decoupling

Beside the capacitive effect of the ground plane under the microcontroller, the fast current has to be delivered from the discrete decoupling capacitors.
Decide for pin-decoupling or/and global decoupling.

4.2.1 Pin-decoupling

Sketch of layout.

By pin-decoupling each pair of V_{DD}-GND pads is first contacted to the capacitor(s) and then to the supply layers/nets. Advantage: Optimised decoupling for every pin possible. Disadvantage: High number of capacitors required.

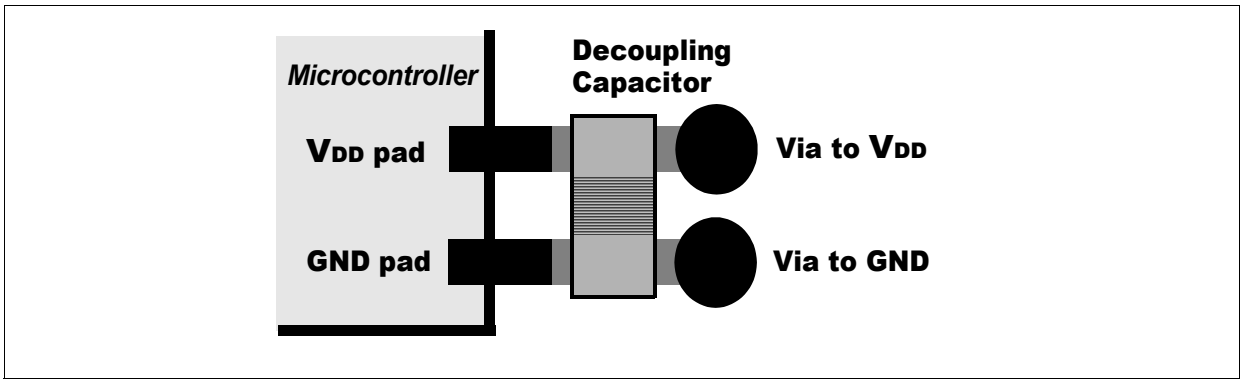

Figure 15 Placing of Blocking Capacitor

Place capacitor-pad as close as possible to the microcontroller's V_{DD}/GND pins.

First contact the capacitor, then contact the vias to GND and V_{DD} plane (see Figure 12).

The connection from the decoupling capacitor to the ground plane can also be realised by several microvias inside the outline of the capacitor pad. That guarantees a low impedant and low inductive connection to ground.

If possible, keep decoupling capacitor on the same side as the MC. Remember vias as additional inductance.

Design traces between pads and capacitor as wide as possible.
.
If you have to place the capacitors on the bottom side of the board provide two or more vias in parallel (think about using microvias) if possible. Keep GND-vias and V_{DD}-vias as close together as possible.

4.2.2 Global Decoupling for Multilayer

Sketch of Layout.
By global decoupling each pair of V_{DD}*-GND pad is first contacted to the supply layers. The capacitors are placed around the MC, directly contacted to the supply plane. Advantage: Lower number of capacitors required since some* V_{DD}*-GND pairs can share one capacitor. Disadvantage: Larger current loops compared to pin-decoupling.*

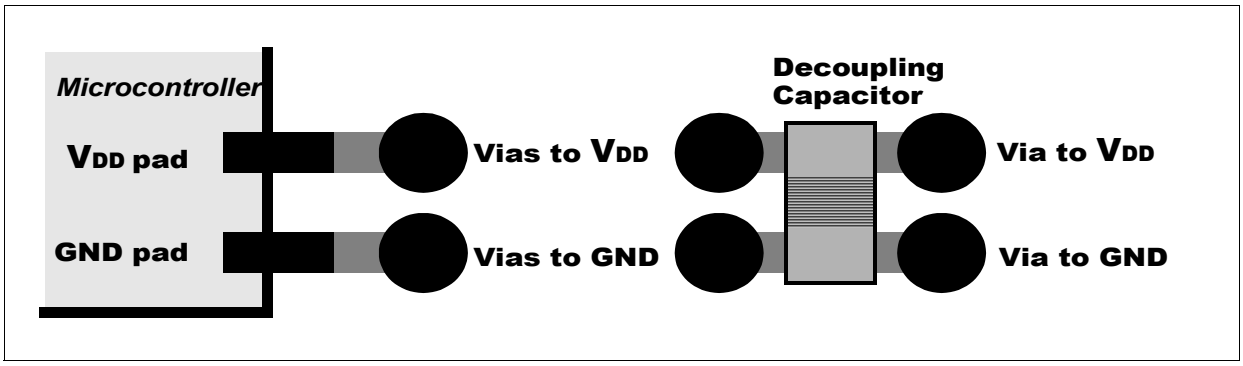

Figure 16 Global Decoupling on Multilayer PCB

Provide at least half as many capacitors of the same value as there are supply pairs at your microcontroller.

Avoid long traces between MC pad and via to supply plane (additional inductance).

Provide two vias in parallel if possible.

Keep GND-vias and V_{DD}-vias as close together as possible.

Note: Global decoupling cannot be used on two layer boards.

Best decoupling concept is a combination of local and global decoupling. This will bring some more costs for discrete components, but can save much development time and redesign activities at critical applications.

4.2.3 Types and Values of Capacitors

Use Surface Mount Device SMD capacitors. This reduces additional lead inductance.

Take care of additional resonant frequencies through decoupling.
This figure shows an equivalent circuit of a decoupled power bus which consists of the capacity of the planes C_{board} on the one side, on the other side there is the equivalent circuit of the decoupling capacitor. This structure is an oscillator with certain resonant frequencies (if one decoupling C is used, then there is just one resonant frequency). If you use two or more values of capacitors, check for additional resonant frequencies.

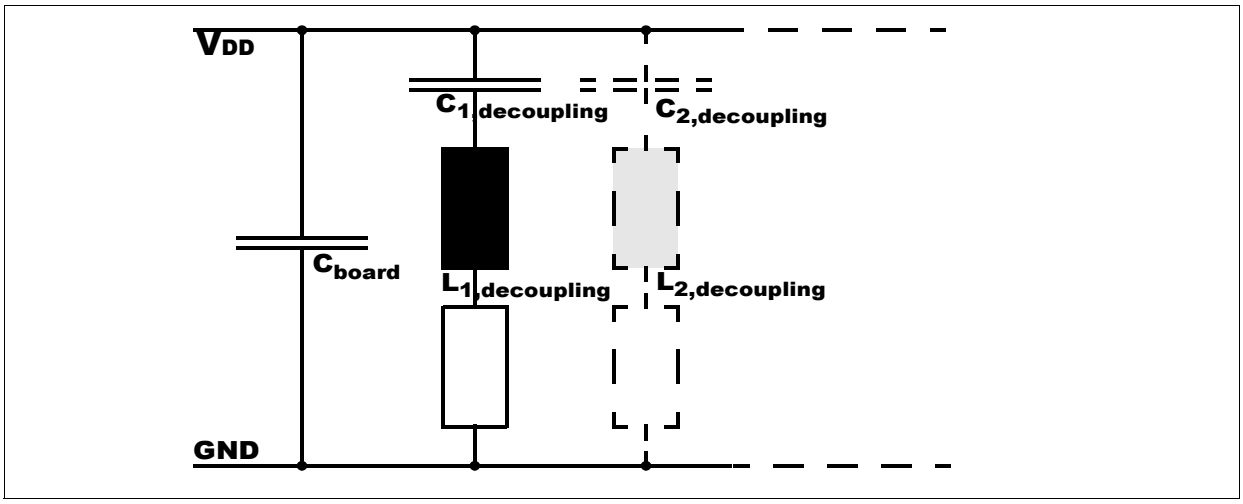

Figure 17 Additional Resonant Frequencies

In general, the suggested value for ceramic capacitors to decouple the power pins of the microcontroller is in the range from 33nF to 100nF. Capacitors have a limited frequency response, which keeps them from delivering power at all the frequencies. Therefore other values of capacitors have to be chosen if special frequencies are of interest.

For global decoupling of the power system, single capacitors in the value range of 33nF up to 100nF are typical. There it is effective to place different values in parallel.

Decoupling at the connectors and the power supply star point (e.g. voltage regulator) should be realised with additional tantalum-electrolyte capacitors.

4.2.4 Damping along Supply-Traces

Since supply systems themselves have their resonance frequency it has to be thought about shifting this resonance out of the range of critical frequencies.
This can be done by shortening the length of the supply trace. In a normal PCB that is not always possible, since board geometries are given from the application functionality. In this case a capacitor in the range of 100nF can be implemented into the current path. This has the effect of shifting the electrical length of the system with the resulting resonance frequency becoming higher.
That means if these capacitors (C1 to Cx) are placed in dedicated distances , e.g. all 3cm to 5cm, along the power trace to ground, the resonance frequency will be above 1GHz. This decoupling principle is based on the various parasitic effects of capacitors at certain frequencies.
This effect is going to be intensified if additional resistors (R1 to Rx) are implemented into the power circuit. *(see Figure 18).* The value of the resistors has to be small, that the capacitor is still working. The exact value has to be specified by test or simulation for the special needs of each application.

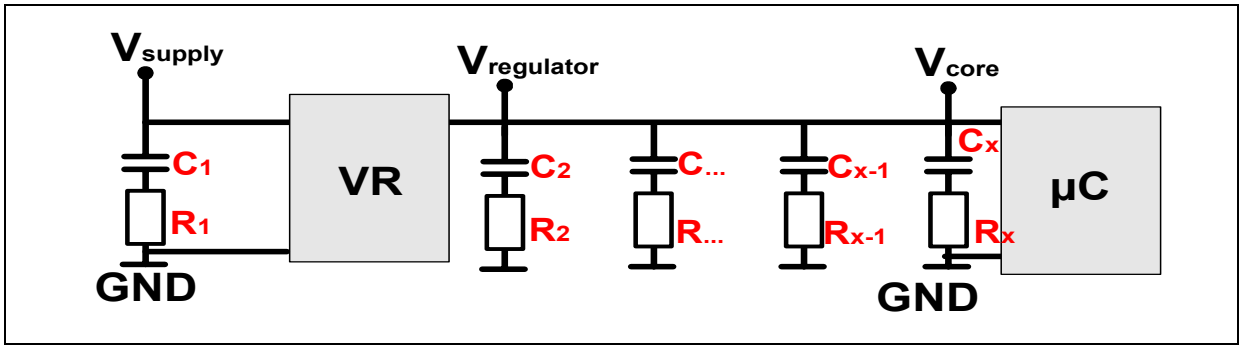

Figure 18 Decoupling of the Power Circuit

5 Further EMC Considerations

Components

For reason of EMS and signal integrity, choose external logic with high input threshold (Vih). E.g. prefer HC (High Speed CMOS) or AC (Advanced CMOS) standard IC's due to higher Vih.
Use the criterion of low cross currents for the selection of other ICs.

Voltage regulator: Canalising of HF Current

To heat transformed or otherwise canalised energy cannot radiate anymore. See an example to position capacitors to isolate and disturb reflected (high frequency) energy. In fact, the high frequency current is created inside the IC. By using blocking capacitors, this HF energy will not leave the circuit via this supply line. But be aware, that energy can couple out via other paths which are connected to the MC.

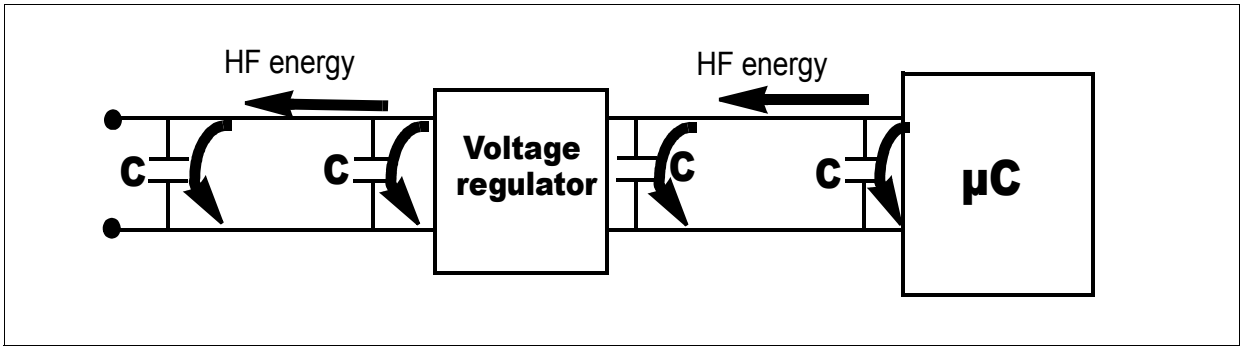

Figure 19 Flow of the Canalised Energy

Vias

For reason of EMC it can be of advantage to use different kinds of vias on a high speed signal application.

Microvias: They have a hole diameter from about 100µm and can be designed into the pads of discrete components. Because of the small diameter much space can be saved on the PCB and therefore the power plane structures are not cut as much as by bigger vias. Because of the same reasons, multiple microvias can be designed instead of one big via. That lowers the inductance of the connection since one can calculate it like inductors in parallel.
Buried vias: This kind of via can be used at a multilayer design. They are connecting some signals or power traces at the inner layers of the PCB (e.g. from the 3rd to the 4th layer) . They are not drilled from top- to bottom layer but just through the inner layers. With buried vias, some layers of a multilayer board can be made high-frequency sealed,

while not cutting the outer planes. Additionally to that space for trace design can be spared.
Blind vias: They are drilled from an outer layer to one of the inner layers. Because of that, not all layers of a PCB are cut for a signal or power trace connection with the first or last few layers. Blind vias are most efficient if used in combination with 'buried vias'.

High impedance traces

By using traces with higher impedance (smaller or narrower traces), disturbances can be kept local. (E.g. traces to the voltage regulator)

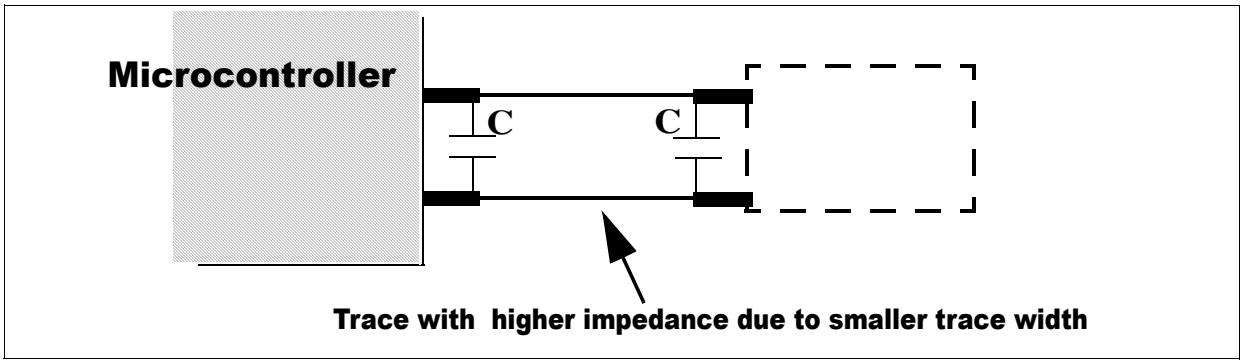

Figure 20 High Impedance Traces

Oscillator

Use lowest speed for oscillator and crystal. Adjust to the demands of the application hardware and software. Use PLL for higher frequencies.
For oscillator and resonator circuit design refer to Application Note INFINEON Technologies 'AP2420xx' and 'AP2424xx'.

Supply Voltage

When a higher supply voltage is used, more power is inside the electrical system. That involves, that a higher voltage fluctuation happens and therefore a higher emission will be created. That means, for the reason of electromagnetic emission, use the lowest possible supply voltage.

If susceptibility is a matter of concern, the supply voltage level should not be too low. A low voltage level implies a small signal-to-noise ratio.

Traces

To avoid EMC disturbances of adjacent traces, try to keep the distance between sensitive traces as big as possible. For high speed signals even guard traces might be necessary. That means, that between two signal traces a ground trace should be designed.

In general, sensitive traces should not be designed in parallel to high speed or noisy traces. If you can not avoid such a design, make the parallel path as short as possible.

Attaching Cables to a PCB

Group connectors by function. E.g. separate analogue cables from high speed signals.

Provide decoupling measures (capacitors, ferrites, optical systems, etc.).

Note: Do not let any noise go from the PCB on the cables since this increases emission dramatically. Do not let any noise go from the cables to the PCB since this may cause functional instabilities.

Provide enough GND pins for a cable transferring critical signals.

Avoid cables if possible. If it is necessary, make them as short as possible. Fix them so they will not move - otherwise their EMC behaviour is unpredictable.

Twist power or signal cables with the corresponding GND cable. Thus, the flow of current and the back current will be close together. Both electromagnetic fields will neutralise each other.

Package

For packages of BGA type, most Vss pins are grouped in the center of the controller. In general the corresponding Vdd pins are located on the inner row of the outer circle. This pinning allows a short connection to the decoupling capacitors, when placed on the opposite side of the PCB.

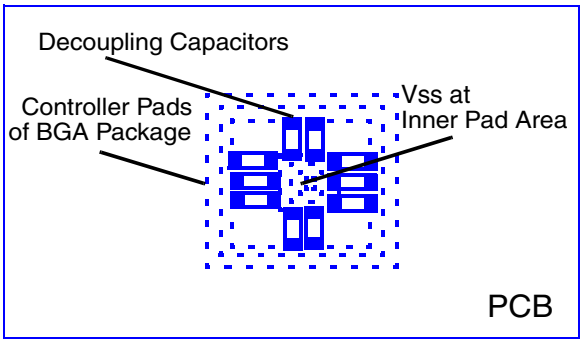

Figure 21

PCB Material

The dielectric permittivity 'ε_{rel}' is important for calculating the wave impedance of a trace or a plane. For the PCB material this constant, at the frequency of 1MHz, can be provided from the board manufacturer. For fast signals it has to be considered that the dielectric permittivity is frequency dependent. (E.g. The material 'FR4' has a ε_{rel} at 1kHz = 4,7 ; At 1MHz = 4,5 ; At 16MHz = 4,35).
In high-speed systems above 4GHz it is recommended to use other materials than the typical 'FR4'. This can be e.g. Teflon or 'BT'-material.

6 Controller Special

16-bit/32-bit Microcontrollers

Dedicated input pins.
These pins, when not used, should be tied up to the level which represents the inactive level for the associated function, e.g. :
$\overline{\text{NMI}}$ (which has no internal pull-up) should be tied to V_{DD}.
$\overline{\text{READY}}$ (which has an internal pull-up) should be tied to V_{DD}.
XTAL3 (input clock for auxiliary oscillator) should be tied to defined level. Because of various types of auxiliary oscillators please specify this level according the Application Note 'AP2420' of Infineon Technologies.

Dedicated output pins.
These pins, when not used, should be left open (e.g. not tied to Vdd or Vss). Connect them to an otherwise unconnected PCB pad for good solderability.

General purpose I/O pins.
When not used, they should be configured by hardware as output. That has functional reasons to prevent a short circuit in case of software mistakes.
These not used I/O pins should then be soldered to pads, which are not connected to any signal or reference plane. This prevents that noise due to internal switching of the microcontroller (ground bouncing) is distributed to the common ground plane.

8-bit Microcontrollers

Take care about routing the ground and power traces at the controller with the corresponding V_{DD} and Vss pins on opposite corners of the controller. If this type of package is used, try to use a global decoupling concept.

Use ALE damping capacitor and resistor for multiplexed address and data pins. Reason for ALE noise at the pin 'P0' is caused by changes from address to data for external access.

7 Simulation

An additional way to improve the design of an application is to test certain structures in the layout by simulation. Find below a description of the most common tools (which are offered by several software manufacturers) and techniques.
By simulation of EMC relevant parameters (like emission, susceptibility and signal-integrity) of electrical systems, an assessment of the necessary effort and the most effective measures can be made. Electrical systems can be: module, printed circuit board (PCB), electrical circuit, sub-circuits and even integrated devices. More and better simulation models are provided from the different manufacturers or distributors. For the 16bit and 32bit microcontrollers from Infineon Technologies, IBIS-models will be provided.

SPICE

Simulation Program with Integrated Circuit Emphasis. SPICE allows the analysis of electrical circuits; for EMI/SI items it allows the analysis of electrical systems (e.g. a bus system) regarding parasitic effects (couplings to neighbouring nets, reflections, etc.). The parasitics themselves are calculated by using a 2-D- or 3-D-Field-solver. The driver and receiver models are supplied by the manufacturers as transistor based models or in the IBIS format. There are plenty of SPICE-like programs.

Generation of SPICE Models

For achieving good results by SPICE simulation, modelling know-how is a basic requirement. The better SPICE models (subcircuits) are, the more efficient analysis becomes. For the analysis of e.g. a bus system, buffer models (mostly provided by the chip manufacturer) and transmission line models (generation by 2D- and 3D-Field-solver) are necessary.

2D-Field-solver Module

A 2D-Field-solver is needed for the determination of the parasitics (capacitance, inductance and resistance values) for (in the 3rd dimension geometrically uniform) transmission lines or transmission line systems, i.e. traces or trace structures. These values can be used to model SPICE subcircuits for the analysis of e.g. bus systems.

3D-Field-solver Module

For more complex structures like vias and rectangular traces, or structures in integrated circuits like packages, wirebonds and leadframe, etc. a 3D-Field-solver is needed to determine the parasitics. Again these values can be used to model SPICE subcircuits.

Emission Module

The electric or magnetic field in any given point in the space around a conducting 3D-structure (especially a PCB) is calculated by adding the corresponding field-vectors caused by all current-vectors of this structure for a given moment in time and given frequency.

Pre-Layout Analysis

Pre-layout analysis means investigation on certain design decisions (even in the specification phase) in order to find an early optimum solution. Pre-layout analysis also means the set-up of a bundle of design-rules for following design stages (i.e. minimum distance of traces to keep crosstalk low, etc.).

Post-Layout Analysis

Post-layout analysis means the investigation (partially/fully) of designed devices (PCBs) in order to detect design hazards, e.g. areas of high EME, before any hardware prototype is built.

8 Formula Appendix

8.A. Calculation of the Characteristic wave impedance of a Microstrip Line

The formulas are valid for a common 'trace over ground-plane' system. Depending on the trace width to dielectrica thickness ratio one of the following formulas is valid.

For narrow traces (trace width / dielectrica thickness < 1):

$$\frac{Z}{\Omega} = \frac{60}{\sqrt{\frac{\varepsilon_{rel}+1}{2}}} * \left[\ln\frac{8h}{w} + \frac{1}{32} * \left(\frac{w}{h}\right)^2 - \frac{1}{2} * \frac{\varepsilon_{rel}-1}{\varepsilon_{rel}+1} * \left(0{,}4516 + \frac{0{,}2416}{\varepsilon_{rel}}\right) \right]$$

For wide traces (trace width / dielectrica thickness > 1) and t/w << 0,1:

$$\frac{Z}{\Omega} = \frac{\frac{188{,}5}{\sqrt{\varepsilon_{rel}}}}{\frac{w}{2h} + 0{,}441 + \frac{\varepsilon_{rel}+1}{2\pi\varepsilon_{rel}} * \left[\ln\left(\frac{w}{2h} + 0{,}94\right) + 1{,}451 \right] + \frac{0{,}082(\varepsilon_{rel}-1)}{\varepsilon_{rel}^{\,2}}}$$

With **h** = height of dielectrica between trace and ground plane; **w** = width of trace; **t** = height of trace.

8.B. Dipole Formula

When a conductor is effective like an antenna, it has a radiated electrical field E of:

This formula is valid, if the length of the conductor (= '**l**') is much smaller and the distance from the conductor (= '**r**') is much larger than the wavelength of the radiation (= 'λ') . '**ZF0**' = the characteristic impedance of free space. 'ϑ '= the angle between the direction of radiation and the axes of the conductor.

8.C. Calculation of Decibel

Decibel [dB] is a dimensionless ratio of power levels. EMC measurement results are expressed in spectrum or limit curves with the unit [dBµV].

Power [dB] = 10 * log(P1/P0), P[dBmW or dBm] = 10 * log(P1/1mW);

(dBm is defined for a 50Ohm system)

with P1 is the measured power, P0 is the reference power.

Voltage [dB] = 20 * log (V1/V0), V[dBµV] = 20 * log(V1/1µV);

with V1 is the measured voltage, V0 is the reference voltage.

(e.g. Harmonic of 100µV amplitude = 20*log(100) = 40 dBµV)

9 Glossary

EMC	Electromagnetic Compatibility (Compatibility regarding emission and susceptibility of electromagnetic disturbances between DUT and environment).
EMI	Electromagnetic Interference (Undesired or illegal generation of electromagnetic signals; bandwidth DC to daylight).
EMS	Electromagnetic Susceptibility (An adverse reaction of electronic equipment to radiated or conducted signals).
EME	Electromagnetic Emission (Radiated or conducted emission of electromagnetic noise by an electronic device).
PCB	Printed circuit board.
DUT	Device Under Test.
HF	High Frequency.
SPICE	Name of a common simulation tool.
IBIS	Input/Output Buffer Information Specification): An emerging standard for electrical behavioural specifications of digital integrated circuit input/output analogue characteristics.
2D Field Solver	Simulation tool for analysis (couplings, characteristic wave impedance, etc.) of two-dimensional trace structures.
3D Field Solver	Simulation tool for analysis (couplings, characteristic wave impedance, etc.) of three-dimensional trace structures like via holes.
SI	Signal Integrity (Reflexion, Timing, Crosstalk).
VI - Table	Static behavioural driver description Voltage vs. Current.
Z_0	Characteristic wave impedance.
XTK	Crosstalk (Interference between two neighbouring traces).
Vih	Threshold current.
Cross (bar) current	Current which flows across two or more transistors connected in line, if they are conducting at the same time.
x-y-tracing	On adjacent signal layers keep traces orthogonal to avoid crosstalk.
ESR	Equivalent Series Resistor of capacitors at high frequency.
ESL	Equivalent Series Inductance of capacitors at high frequency.
Microvia	Via with a diameter of about 100µm.

10 Literature

For more detailed information and physical explanations it might be useful to have a book or lecture about the subject of EMC. The following list is a selection of literature which includes the various subjects of EMC, like emission, susceptibility and electrostatic discharge.

- A.Schwab, **Elektromagnetische Verträglichkeit**, 3.Ausgabe, Springer Verlag, 1994 Berlin-Heidelberg. (German language). [commentary: Good book for wide basic knowledge of EMC] ISBN: 3-540-57658-4

- Michael Mardiguian, **Controlling Radiated Emission by Design**, Chapman & Hall, 1992 New York, [commentary: detailed and special for radiation] ISBN: 0-442-00949-6

- Howard Johnson, Martin Graham, **High-Speed Digital Design - A Handbook of Black Magic**, 1993 by Prentice Hall PTR. [commentary: very detailed and mathematical] ISBN: 0-13-395724-1

- Mark Montrose: **EMC and the Printed Circuit Board: Design, Theory and Layout Made Simple**, IEEE Electromagnetic Compatibility Society IEEE, [Contents: EMC Fundamentals; EMC inside the PCB; Components and EMC; Image Planes; Bypassing and Decoupling; Transmission Lines; Signal Integrity and Crosstalk; Grounding Concept.] ISBN 0-7803-4703-X

- **EMC KOMPENDIUM 1999 - 2000**, publish-industry Verlag GmbH, Munich, (in German) E-mail: info@kmverlag.de or fosjames@erols.com.

- Paper to the workshop "Optimized Decoupling Concepts for Digital VLSI Circuits", Joachim Held, Siemens AG I&S ITPS8 Munich; Prof. Thomas Wolf, University of Applied Sciences, Landshut; IEEE - EMC seminar 2001

- **Paper to the seminar "EMV auf Leiterplatten 1999"**, Prof. Chr. Dirks, puplished by Nils Dirks Corporate Consulting, Donaueschingen. (German language)

- **Paper to the workshop "EMV auf Leiterplattenebene"**, Werner John, MESAGO GmbH Stuttgart. (German language)

- Paper to the workshop "Techniques for PCB and Circuit Level Radiation Reduction", David A. Weston, MESAGO GmbH Stuttgart.

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Dr. Ulrich Schumacher

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