AN1001

Fundamental Characteristics of Thyristors

Introduction

The thyristor family of semiconductors consists of several very useful devices. The most widely used of this family are silicon controlled rectifiers (SCRs), triacs, sidacs, and diacs. In many applications these devices perform key functions and are real assets in meeting environmental, speed, and reliability specifications which their electro-mechanical counterparts cannot fulfill.

This application note presents the basic fundamentals of SCR, triac, sidac, and diac thyristors so the user understands how they differ in characteristics and parameters from their electro-mechanical counterparts. Also, thyristor terminology is defined.

SCR

Basic Operation

Figure AN1001.1 shows the simple block construction of an SCR.

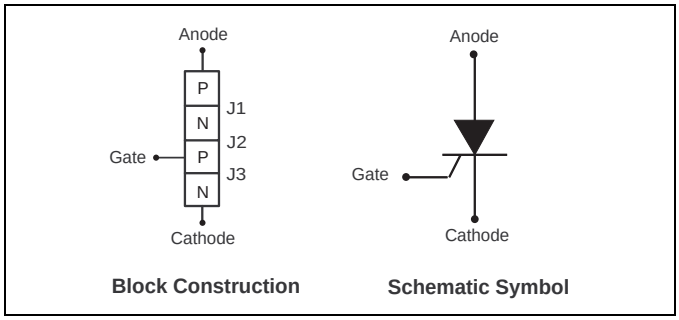


Figure AN1001.1 SCR Block Construction

The operation of a PNPN device can best be visualized as a specially coupled pair of transistors as shown in Figure AN1001.2.

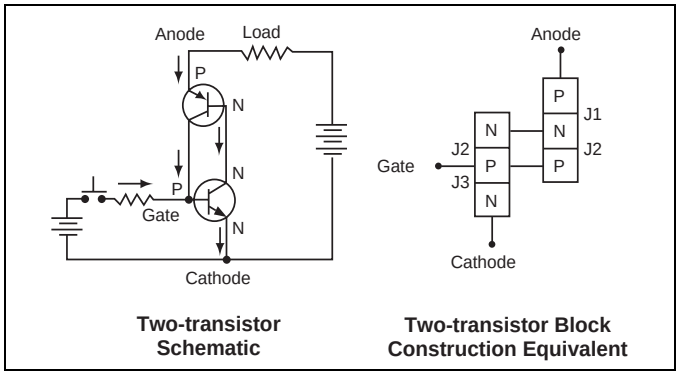


Figure AN1001.2 Coupled Pair of Transistors as a SCR

The connections between the two transistors trigger the occurrence of regenerative action when a proper gate signal is applied to the base of the NPN transistor. Normal leakage current is so low that the combined h_{FE} of the specially coupled two-transistor feedback amplifier is less than unity, thus keeping the circuit in an off-state condition. A momentary positive pulse applied to the gate biases the NPN transistor into conduction which, in turn, biases the PNP transistor into conduction. The effective h_{FE} momentarily becomes greater than unity so that the specially coupled transistors saturate. Once saturated, current through the transistors is enough to keep the combined h_{FE} greater than unity. The circuit remains “on” until it is “turned off” by reducing the anode-to-cathode current (I_T) so that the combined h_{FE} is less than unity and regeneration ceases. This threshold anode current is the holding current of the SCR.

Geometric Construction

Figure AN1001.3 shows cross-sectional views of an SCR chip and illustrations of current flow and junction biasing in both the blocking and triggering modes.

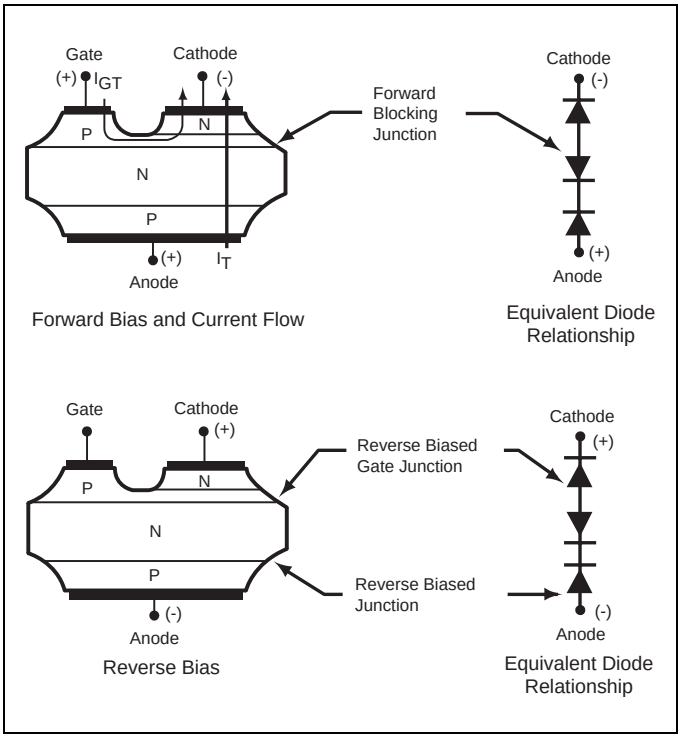


Figure AN1001.3 Cross-sectional View of SCR Chip

Triac

Basic Operation

Figure AN1001.4 shows the simple block construction of a triac. Its primary function is to control power bilaterally in an AC circuit.

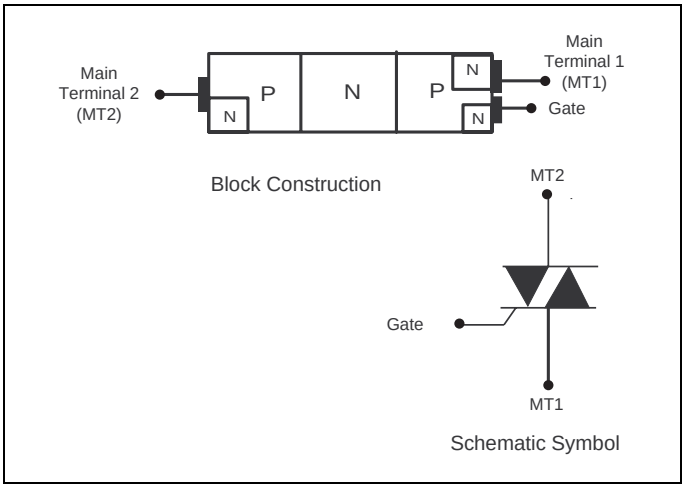


Figure AN1001.4 Triac Block Construction

Operation of a triac can be related to two SCRs connected in parallel in opposite directions as shown in Figure AN1001.5.

Although the gates are shown separately for each SCR, a triac has a single gate and can be triggered by either polarity.

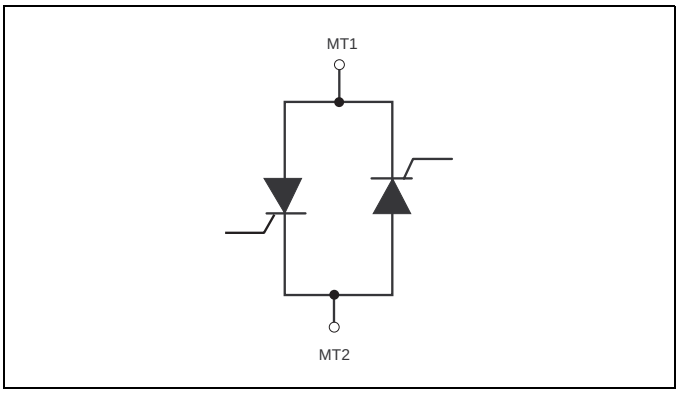


Figure AN1001.5 SCRs Connected as a Triac

Since a triac operates in both directions, it behaves essentially the same in either direction as an SCR would behave in the forward direction (blocking or operating).

Geometric Construction

Figure AN1001.6 show simplified cross-sectional views of a triac chip in various gating quadrants and blocking modes.

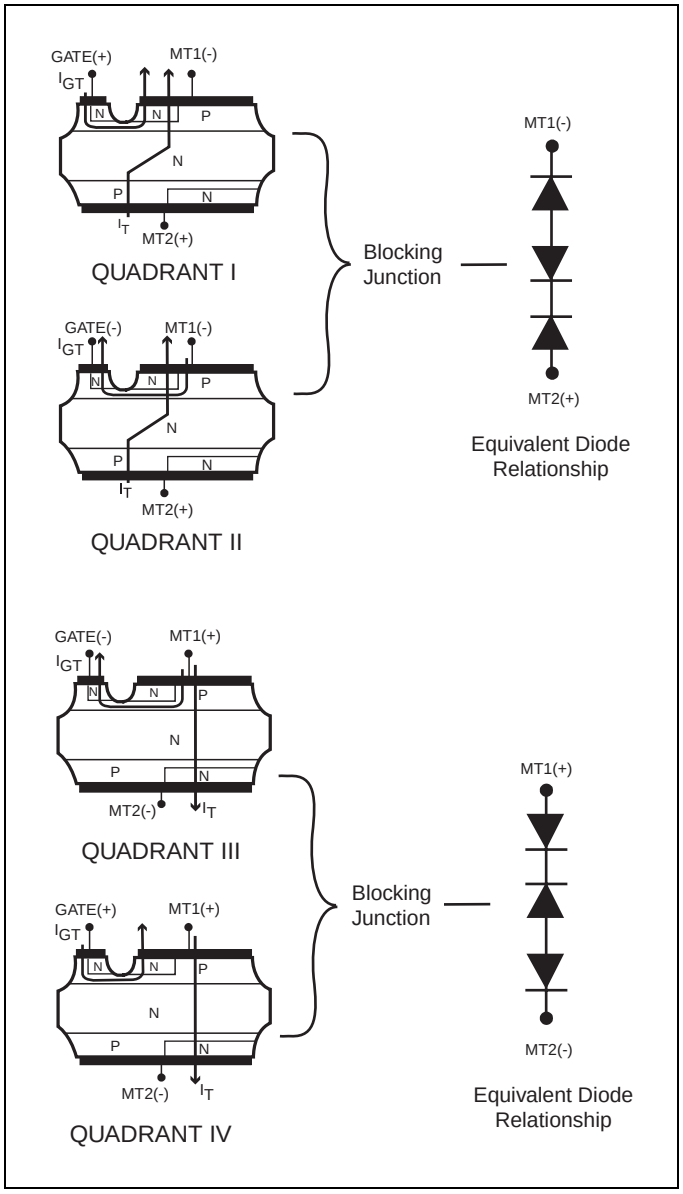


Figure AN1001.6 Simplified Cross-sectional of Triac Chip

Sidac

Basic Operation

The sidac is a multi-layer silicon semiconductor switch. Figure AN1001.7 illustrates its equivalent block construction using two Shockley diodes connected inverse parallel. Figure AN1001.7 also shows the schematic symbol for the sidac.

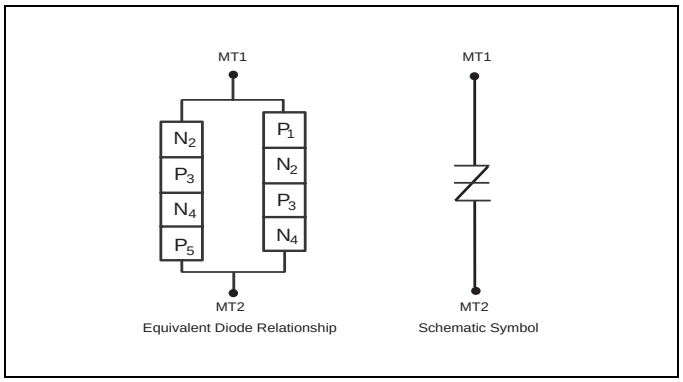


Figure AN1001.7 Sidac Block Construction

The sidac operates as a bidirectional switch activated by voltage. In the off state, the sidac exhibits leakage currents (I_{DRM}) less than 5 µA. As applied voltage exceeds the sidac V_{BO}, the device begins to enter a negative resistance switching mode with characteristics similar to an avalanche diode. When supplied with enough current (I_S), the sidac switches to an on state, allowing high current to flow. When it switches to on state, the voltage across the device drops to less than 5 V, depending on magnitude of the current flow. When the sidac switches on and drops into regeneration, it remains on as long as holding current is less than maximum value (150 mA, typical value of 30 mA to 65 mA). The switching current (I_S) is very near the holding current (I_H) value. When the sidac switches, currents of 10 A to 100 A are easily developed by discharging small capacitor into primary or small, very high-voltage transformers for 10 µs to 20 µs.

The main application for sidacs is ignition circuits or inexpensive high voltage power supplies.

Geometric Construction

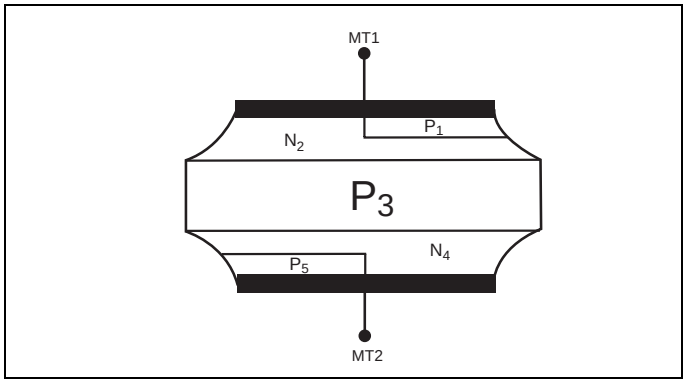


Figure AN1001.8 Cross-sectional View of a Bidirectional Sidac Chip with Multi-layer Construction

Diac

Basic Operation

The construction of a diac is similar to an open base NPN transistor. Figure AN1001.9 shows a simple block construction of a diac and its schematic symbol.

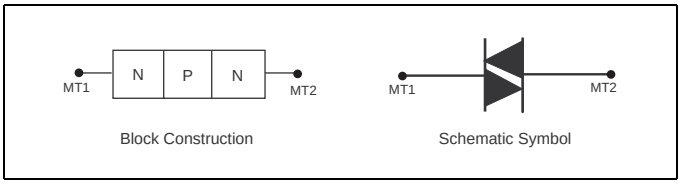


Figure AN1001.9 Diac Block Construction

The bidirectional transistor-like structure exhibits a high-impedance blocking state up to a voltage breakover point (V_{BO}) above which the device enters a negative-resistance region. These basic diac characteristics produce a bidirectional pulsing oscillator in a resistor-capacitor AC circuit. Since the diac is a bidirectional device, it makes a good economical trigger for firing triacs in phase control circuits such as light dimmers and motor speed controls. Figure AN1001.10 shows a simplified AC circuit using a diac and a triac in a phase control application.

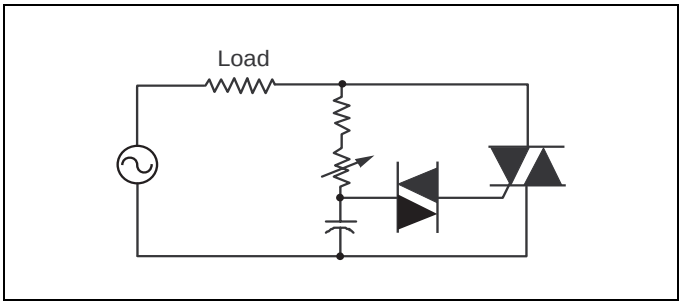


Figure AN1001.10 AC Phase Control Circuit

Geometric Construction

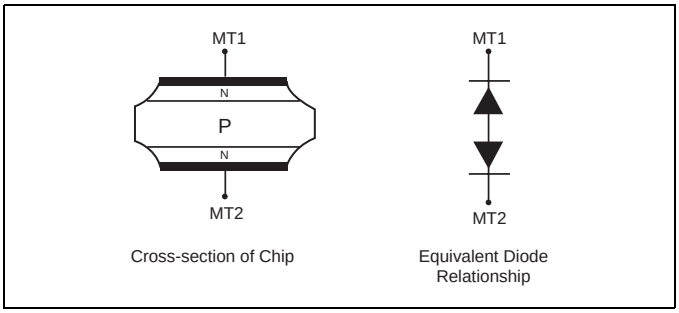


Figure AN1001.11 Cross-sectional View of Diac Chip

Electrical Characteristic Curves of Thyristors

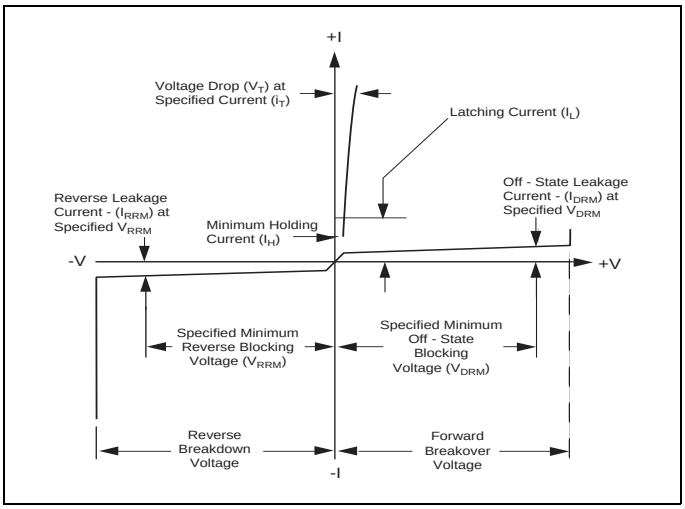


Figure AN1001.12 V-I Characteristics of SCR Device

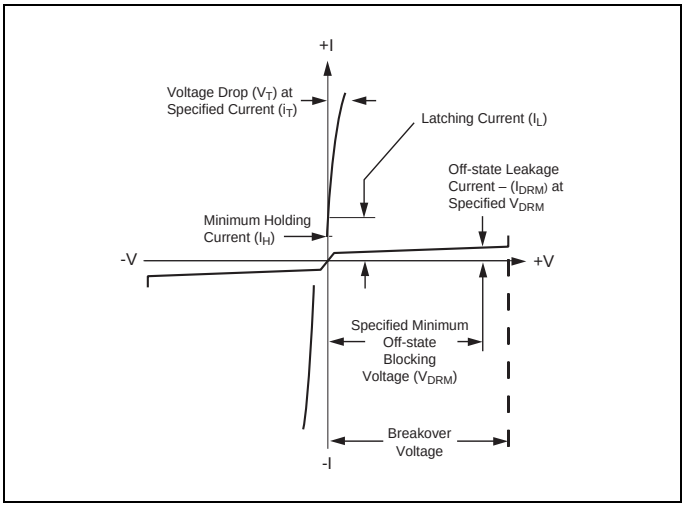


Figure AN1001.13 V-I Characteristics of Triac Device

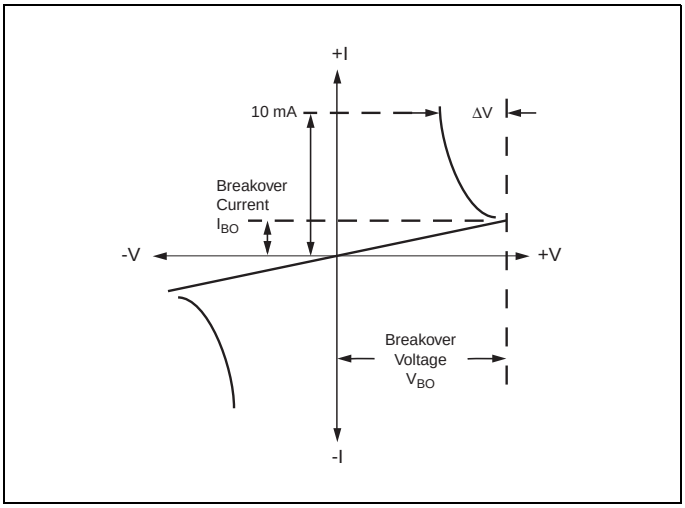


Figure AN1001.14 V-I Characteristics of Bilateral Trigger Diac

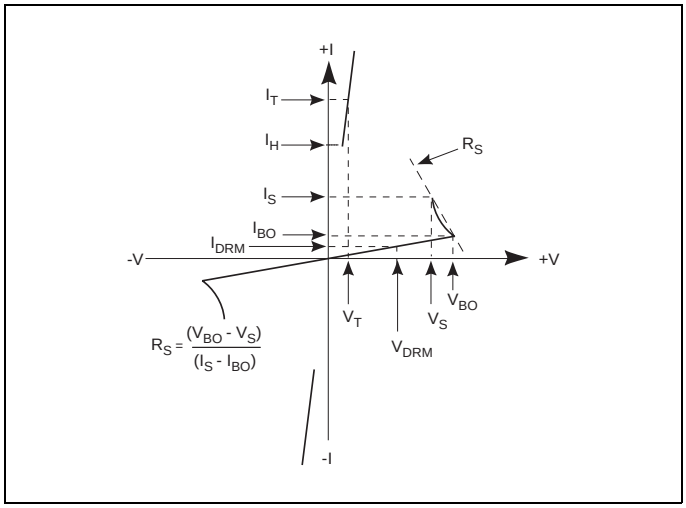


Figure AN1001.15 V-I Characteristics of a Sidac Chip

Methods of Switching on Thyristors

Three general methods are available for switching thyristors to on-state condition:

- Application of gate signal
- Static dv/dt turn-on
- Voltage breakover turn-on

Application Of Gate Signal

Gate signal must exceed I_{GT} and V_{GT} requirements of the thyristor used. For an SCR (unilateral device), this signal must be positive with respect to the cathode polarity. A triac (bilateral device) can be turned on with gate signal of either polarity; however, different polarities have different requirements of I_{GT} and V_{GT} which must be satisfied. Since diacs and sidacs do not have a gate, this method of turn-on is not applicable. In fact, the single major application of diacs is to switch on triacs.

Static dv/dt Turn-on

Static dv/dt turn-on comes from a fast-rising voltage applied across the anode and cathode terminals of an SCR or the main terminals of a triac. Due to the nature of thyristor construction, a small junction capacitor is formed across each PN junction. Figure AN1001.16 shows how typical internal capacitors are linked in gated thyristors.

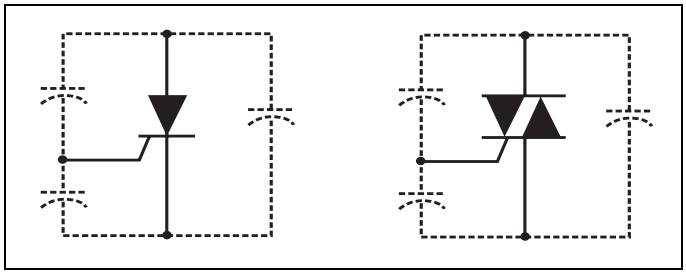


Figure AN1001.16 Internal Capacitors Linked in Gated Thyristors

When voltage is impressed suddenly across a PN junction, a charging current flows, equal to:

$$i = C\left(\frac{dv}{dt}\right)$$

When $C\left(\frac{dv}{dt}\right)$ becomes greater or equal to thyristor I_{GT},

the thyristor switches on. Normally, this type of turn-on does not damage the device, providing the surge current is limited.

Generally, thyristor application circuits are designed with static dv/dt snubber networks if fast-rising voltages are anticipated.

Voltage Breakover Turn-on

This method is used to switch on sidacs and diacs. However, exceeding voltage breakover of SCRs and triacs is definitely not recommended as a turn-on method.

In the case of SCRs and triacs, leakage current increases until it exceeds the gate current required to turn on these gated thyristors in a small localized point. When turn-on occurs by this method, localized heating in a small area may melt the silicon or damage the device if di/dt of the increasing current is not sufficiently limited.

Diacs used in typical phase control circuits are basically protected against excessive current at breakover as long as the firing capacitor is not excessively large. When diacs are used in a zener function, current limiting is necessary.

Sidacs are typically pulse-firing, high-voltage transformers and are current limited by the transformer primary. The sidac should be operated so peak current amplitude, current duration, and di/dt limits are not exceeded.

Triac Gating Modes Of Operation

Triacs can be gated in four basic gating modes as shown in Figure AN1001.17.

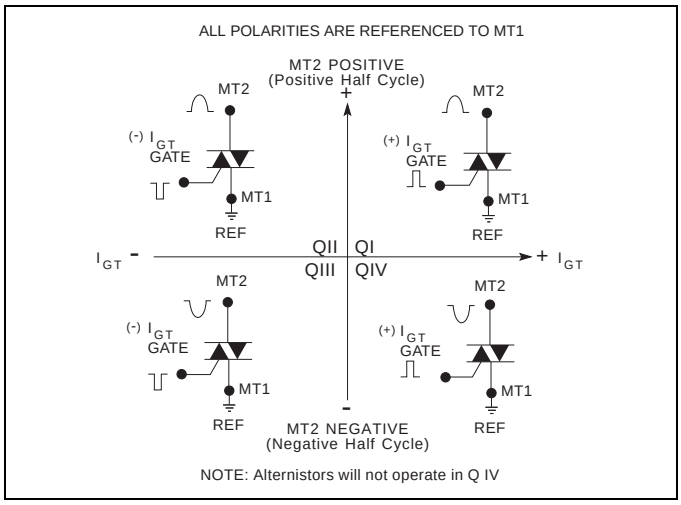


Figure AN1001.17 Gating Modes

The most common quadrants for triac gating-on are Quadrants I and III, where the gate supply is synchronized with the main terminal supply (gate positive — MT2 positive, gate negative — MT2 negative). Gate sensitivity of triacs is most optimum in Quadrants I and III due to the inherent thyristor chip construction. If Quadrants I and III cannot be used, the next best operating modes are Quadrants II and III where the gate has a negative polarity supply with an AC main terminal supply. Typically, Quadrant II is approximately equal in gate sensitivity to Quadrant I; however, latching current sensitivity in Quadrant II is lowest. Therefore, it is difficult for triacs to latch on in Quadrant II when the main terminal current supply is very low in value.

Special consideration should be given to gating circuit design when Quadrants I and IV are used in actual application, because Quadrant IV has the lowest gate sensitivity of all four operating quadrants.

General Terminology

The following definitions of the most widely-used thyristor terms, symbols, and definitions conform to existing EIA-JEDEC standards:

Breakover Point – Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value

Principal Current – Generic term for the current through the collector junction (the current through main terminal 1 and main terminal 2 of a triac or anode and cathode of an SCR)

Principal Voltage – Voltage between the main terminals:

(1) In the case of reverse blocking thyristors, the principal voltage is called positive when the anode potential is higher than the cathode potential and negative when the anode potential is lower than the cathode potential.

(2) For bidirectional thyristors, the principal voltage is called positive when the potential of main terminal 2 is higher than the potential of main terminal 1.

Off State – Condition of the thyristor corresponding to the high-resistance, low-current portion of the principal voltage-current characteristic between the origin and the breakover point(s) in the switching quadrant(s)

On State – Condition of the thyristor corresponding to the low-resistance, low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).

Specific Terminology

Average Gate Power Dissipation [$P_{G(AV)}$] – Value of gate power which may be dissipated between the gate and main terminal 1 (or cathode) averaged over a full cycle

Breakover Current (I_{BO}) – Principal current at the breakover point

Breakover Voltage (V_{BO}) – Principal voltage at the breakover point

Circuit-commutated Turn-off Time (t_q) – Time interval between the instant when the principal current has decreased to zero after external switching of the principal voltage circuit and the instant when the thyristor is capable of supporting a specified principal voltage without turning on

Critical Rate-of-rise of Commutation Voltage of a Triac (Commutating dv/dt) – Minimum value of the rate-of-rise of principal voltage which will cause switching from the off state to the on state immediately following on-state current conduction in the opposite quadrant

Critical Rate-of-rise of Off-state Voltage or Static dv/dt (dv/dt) – Minimum value of the rate-of-rise of principal voltage which will cause switching from the off state to the on state

Critical Rate-of-rise of On-state Current (di/dt) – Maximum value of the rate-of-rise of on-state current that a thyristor can withstand without harmful effect

Gate-controlled Turn-on Time (t_{gt}) – Time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped to a specified low value (or risen to a specified high value) during switching of a thyristor from off state to the on state by a gate pulse.

Gate Trigger Current (I_{GT}) – Minimum gate current required to maintain the thyristor in the on state

Gate Trigger Voltage (V_{GT}) – Gate voltage required to produce the gate trigger current

Holding Current (I_H) – Minimum principal current required to maintain the thyristor in the on state

Latching Current (I_L) – Minimum principal current required to maintain the thyristor in the on state immediately after the switching from off state to on state has occurred and the triggering signal has been removed

On-state Current (I_T) – Principal current when the thyristor is in the on state

On-state Voltage (V_T) – Principal voltage when the thyristor is in the on state

Peak Gate Power Dissipation (P_{GM}) – Maximum power which may be dissipated between the gate and main terminal 1 (or cathode) for a specified time duration

Repetitive Peak Off-state Current (I_{DRM}) – Maximum instantaneous value of the off-state current that results from the application of repetitive peak off-state voltage

Repetitive Peak Off-state Voltage (V_{DRM}) – Maximum instantaneous value of the off-state voltage which occurs across a thyristor, including all repetitive transient voltages and excluding all non-repetitive transient voltages

Repetitive Peak Reverse Current of an SCR (I_{RRM}) – Maximum instantaneous value of the reverse current resulting from the application of repetitive peak reverse voltage

Repetitive Peak Reverse Voltage of an SCR (V_{RRM}) – Maximum instantaneous value of the reverse voltage which occurs across the thyristor, including all repetitive transient voltages and excluding all non-repetitive transient voltages

Surge (Non-repetitive) On-state Current (I_{TSM}) – On-state current of short-time duration and specified waveshape

Thermal Resistance, Junction to Ambient ($R_{\theta JA}$) – Temperature difference between the thyristor junction and ambient divided by the power dissipation causing the temperature difference under conditions of thermal equilibrium

Note: Ambient is the point at which temperature does not change as the result of dissipation.

Thermal Resistance, Junction to Case ($R_{\theta JC}$) – Temperature difference between the thyristor junction and the thyristor case divided by the power dissipation causing the temperature difference under conditions of thermal equilibrium

AN1002

Gating, Latching, and Holding of SCRs and Triacs

Introduction

Gating, latching, and holding currents of thyristors are some of the most important parameters. These parameters and their interrelationship determine whether the SCRs and triacs will function properly in various circuit applications.

This application note describes how the SCR and triac parameters are related. This knowledge helps users select best operating modes for various circuit applications.

Gating of SCRs and Triacs

Three general methods are available to switch thyristors to on-state condition:

- Applying proper gate signal
- Exceeding thyristor static dv/dt characteristics
- Exceeding voltage breakover point

This application note examines only the application of proper gate signal. Gate signal must exceed the I_{GT} and V_{GT} requirements of the thyristor being used. I_{GT} (gate trigger current) is the minimum gate current required to switch a thyristor from the off state to the on state. V_{GT} (gate trigger voltage) is the voltage required to produce the gate trigger current.

SCRs (unilateral devices) require a positive gate signal with respect to the cathode polarity. Figure AN1002.1 shows the current flow in a cross-sectional view of the SCR chip.

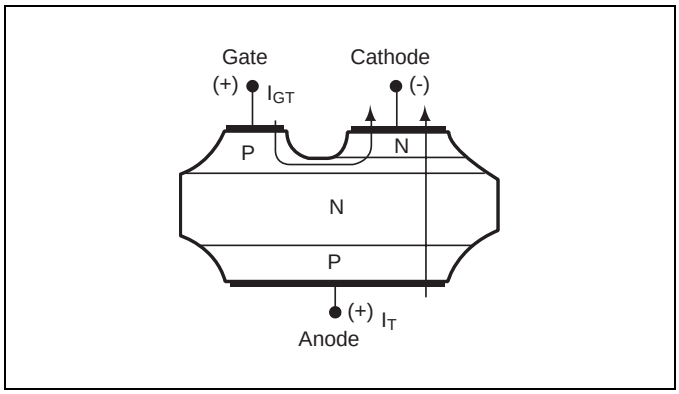


Figure AN1002.1 SCR Current Flow

In order for the SCR to latch on, the anode-to-cathode current (I_T) must exceed the latching current (I_L) requirement. Once latched on, the SCR remains on until it is turned off when anode-to-cathode current drops below holding current (I_H) requirement.

Triacs (bilateral devices) can be gated on with a gate signal of either polarity with respect to the MT1 terminal; however, different polarities have different requirements of I_{GT} and V_{GT}. Figure AN1002.2 illustrates current flow through the triac chip in various gating modes.

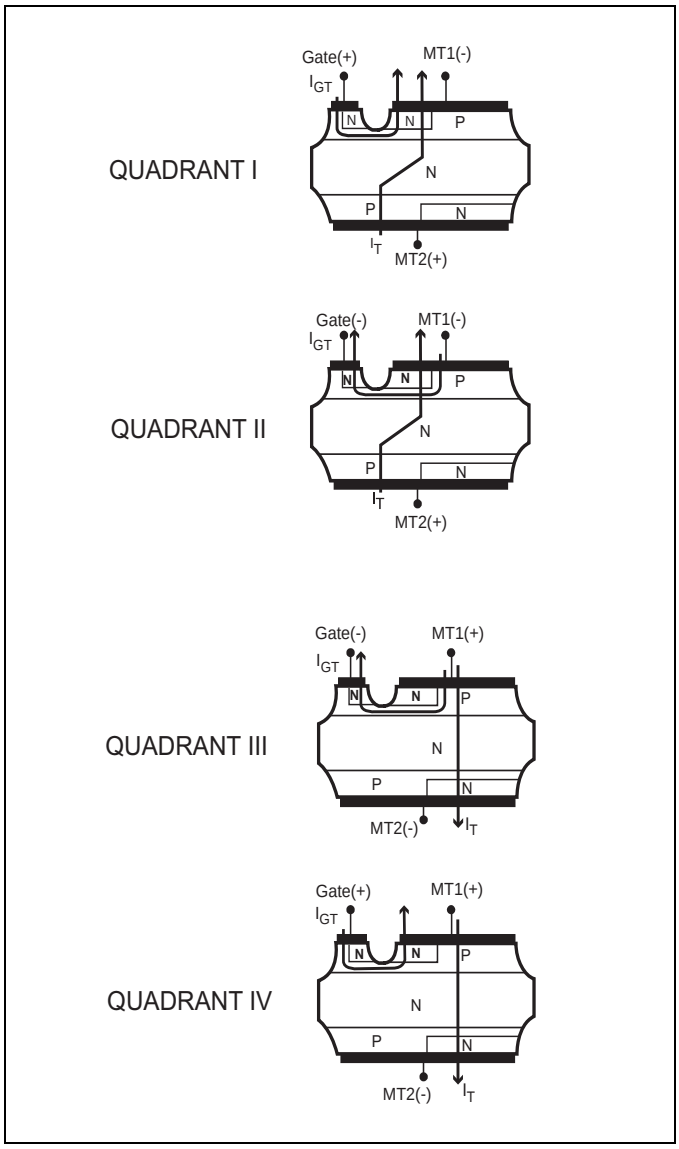


Figure AN1002.2 Triac Current Flow (Four Operating Modes)

Triacs can be gated on in one of four basic gating modes as shown in Figure AN1002.3. The most common quadrants for gating on triacs are Quadrants I and III, where the gate supply is synchronized with the main terminal supply (gate positive — MT2 positive, gate negative — MT2 negative). Optimum triac gate sensitivity is achieved when operating in Quadrants I and III due to the inherent thyristor chip construction. If Quadrants I and III cannot be used, the next best operating modes are Quadrants II and III where the gate supply has a negative polarity with an AC main terminal supply. Typically, Quadrant II is approximately equal in gate sensitivity to Quadrant I; however, latching current sensitivity in Quadrant II is lowest. Therefore, it is difficult for triacs to latch on in Quadrant II when the main terminal current supply is very low in value.

Special consideration should be given to gating circuit design when Quadrants I and IV are used in actual application, because Quadrant IV has the lowest gate sensitivity of all four operating quadrants.

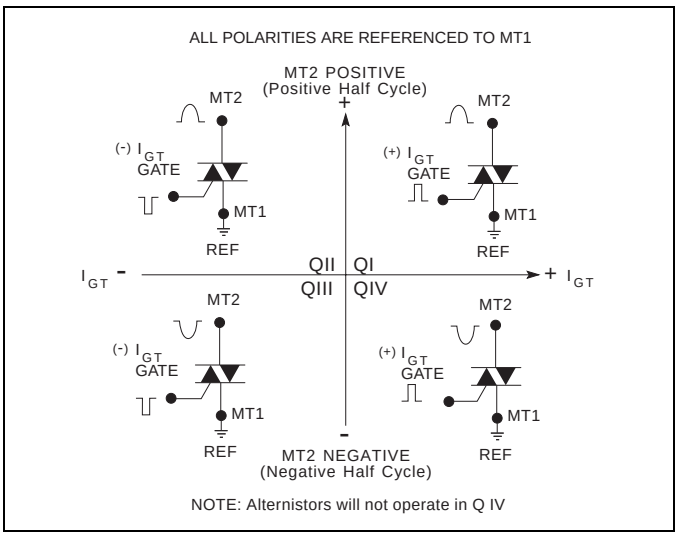


Figure AN1002.3 Definition of Operating Quadrants in Triacs

The following table shows the relationships between different gating modes in current required to gate on triacs.

Typical Ratio of $\frac{I_{GT}(\text{In given Quadrant})}{I_{GT}(\text{Quadrant 1})}$ at 25 °C				
Type	Operating Mode			
	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
4 A Triac	1	1.6	2.5	2.7
10 A Triac	1	1.5	1.4	3.1

Example of 4 A triac:

If $I_{GT}(I)$ = 10 mA, then
$I_{GT}(II)$ = 16 mA
$I_{GT}(III)$ = 25 mA
$I_{GT}(IV)$ = 27 mA

Gate trigger current is temperature-dependent as shown in Figure AN1002.4. Thyristors become less sensitive with decreasing temperature and more sensitive with increasing temperature.

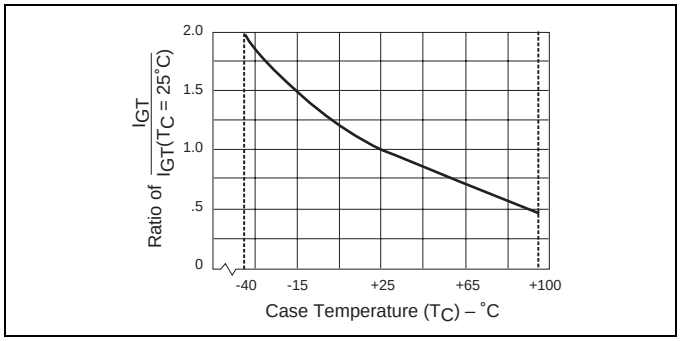


Figure AN1002.4 Typical DC Gate Trigger Current versus Case Temperature

For applications where low temperatures are expected, gate current supply should be increased to at least two to eight times the gate trigger current requirements at 25 °C. The actual factor varies by thyristor type and the environmental temperature.

Example of a 10 A triac:

If $I_{GT}(I)$ = 10 mA at 25 °C, then
$I_{GT}(I)$ = 20 mA at -40 °C

In applications where high di/dt, high surge, and fast turn-on are expected, gate drive current should be steep rising (1 µs rise time) and at least twice rated I_{GT} or higher with minimum 3 µs pulse duration. However, if gate drive current magnitude is very high, then duration may have to be limited to keep from overstressing (exceeding the power dissipation limit of) gate junction.

Latching Current of SCRs and Triacs

Latching current (I_L) is the minimum principal current required to maintain the thyristor in the on state immediately after the switching from off state to on state has occurred and the triggering signal has been removed. Latching current can best be understood by relating to the “pick-up” or “pull-in” level of a mechanical relay. Figure AN1002.5 and Figure AN1002.6 illustrate typical thyristor latching phenomenon.

In the illustrations in Figure AN1002.5, the thyristor does not stay on after gate drive is removed due to insufficient available principal current (which is lower than the latching current requirement).

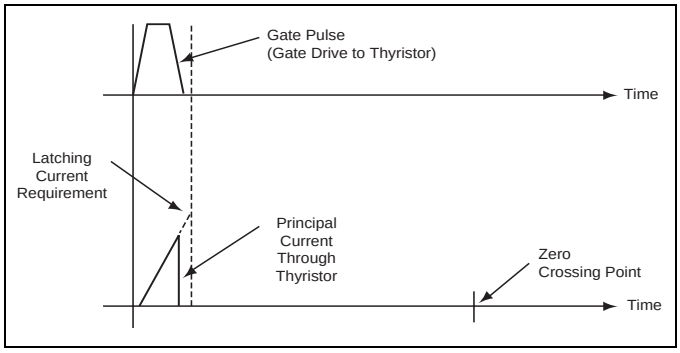


Figure AN1002.5 Latching Characteristic of Thyristor (Device Not Latched)

In the illustration in Figure AN1002.6 the device stays on for the remainder of the half cycle until the principal current falls below the holding current level. Figure AN1002.5 shows the characteristics of the same device if gate drive is removed or shortened before latching current requirement has been met.

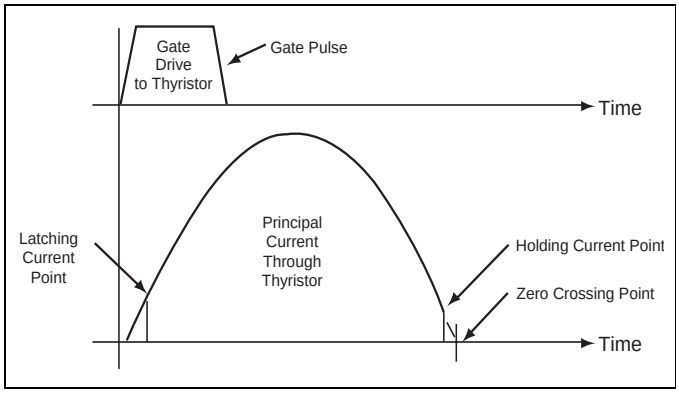


Figure AN1002.6 Latching and Holding Characteristics of Thyristor

Similar to gating, latching current requirements for triacs are different for each operating mode (quadrant). Definitions of latching modes (quadrants) are the same as gating modes. Therefore, definitions shown in Figure AN1002.2 and Figure AN1002.3 can be used to describe latching modes (quadrants) as well. The following table shows how different latching modes (quadrants) relate to each other. As previously stated, Quadrant II has the lowest latching current sensitivity of all four operating quadrants.

Typical Ratio of $\frac{I_L(In\ given\ Quadrant)}{I_L(Quadrant\ 1)}$ at 25 °C				
	Operating Mode			
Type	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
4 A Triac	1	4	1.2	1.1
10 A Triac	1	4	1.1	1

Example of a 4 Amp Triac:

If $I_L(I)$ = 10 mA, then
$I_L(II)$ = 40 mA
$I_L(III)$ = 12 mA
$I_L(IV)$ = 11 mA

Latching current has even somewhat greater temperature dependence compared to the DC gate trigger current. Applications with low temperature requirements should have sufficient principal current (anode current) available to ensure thyristor latch-on.

Two key test conditions on latching current specifications are gate drive and available principal (anode) current durations. Shortening the gate drive duration can result in higher latching current values.

Holding Current of SCRs and Triacs

Holding current (I_H) is the minimum principal current required to maintain the thyristor in the on state. Holding current can best be understood by relating it to the “drop-out” or “must release” level of a mechanical relay. Figure AN1002.6 shows the sequences of gate, latching, and holding currents. Holding current will always be less than latching. However, the more sensitive the device, the closer the holding current value approaches its latching current value.

Holding current is independent of gating and latching, but the device must be fully latched on before a holding current limit can be determined.

Holding current modes of the thyristor are strictly related to the voltage polarity across the main terminals. The following table illustrates how the positive and negative holding current modes of triacs relate to each other.

Typical Triac Holding Current Ratio		
	Operating Mode	
Type	$I_H(+)$	$I_H(-)$
4 A Triac	1	1.1
10 A Triac	1	1.3

Example of a 10 A triac:

If $I_H(+)$ = 10 mA, then
$I_H(-)$ = 13 mA

Holding current is also temperature-dependent like gating and latching shown in Figure AN1002.7. The initial on-state current is 200 mA to ensure that the thyristor is fully latched on prior to holding current measurement. Again, applications with low temperature requirements should have sufficient principal (anode) current available to maintain the thyristor in the on-state condition.

Both minimum and maximum holding current specifications may be important, depending on application. Maximum holding current must be considered if the thyristor is to stay in conduction at low principal (anode) current; the minimum holding current must be considered if the device is expected to turn off at a low principal (anode) current.

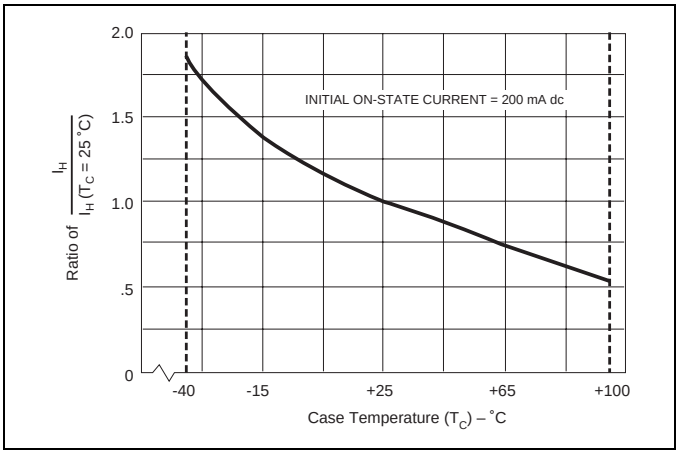


Figure AN1002.7 Typical DC Holding Current vs Case Temperatures

Example of a 10 A triac:

If $I_H(+)$ = 10 mA at 25 °C, then
$I_H(+) \approx$ 7.5 mA at 65 °C

Relationship of Gating, Latching, and Holding Currents

Although gating, latching, and holding currents are independent of each other in some ways, the parameter values are related. If gating is very sensitive, latching and holding will also be very sensitive and vice versa. One way to obtain a sensitive gate and not-so-sensitive latching-holding characteristic is to have an “amplified gate” as shown in Figure AN1002.8.

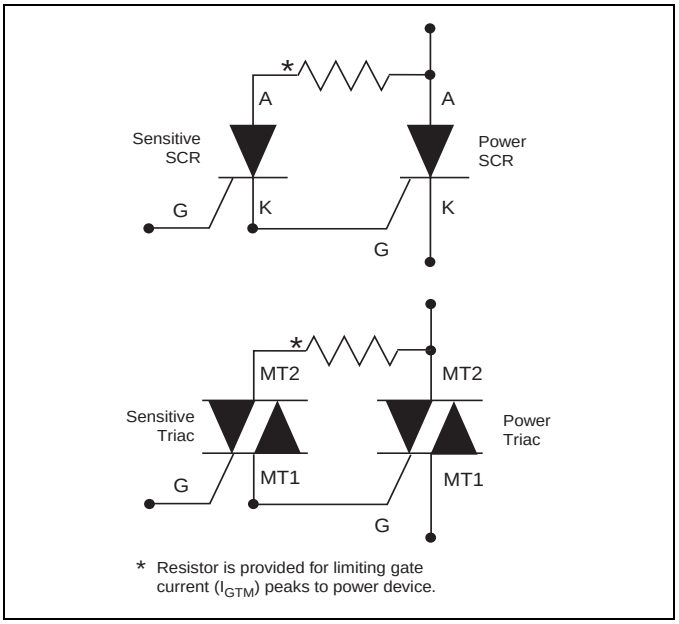


Figure AN1002.8 "Amplified Gate" Thyristor Circuit

The following table and Figure AN1002.9 show the relationship of gating, latching, and holding of a 4 A device.

Typical 4 A Triac Gating, Latching, and Holding Relationship				
	Quadrants or Operating Mode			
Parameter	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
I_{GT} (mA)	10	17	18	27
I_L (mA)	12	48	12	13
I_H (mA)	10	10	12	12

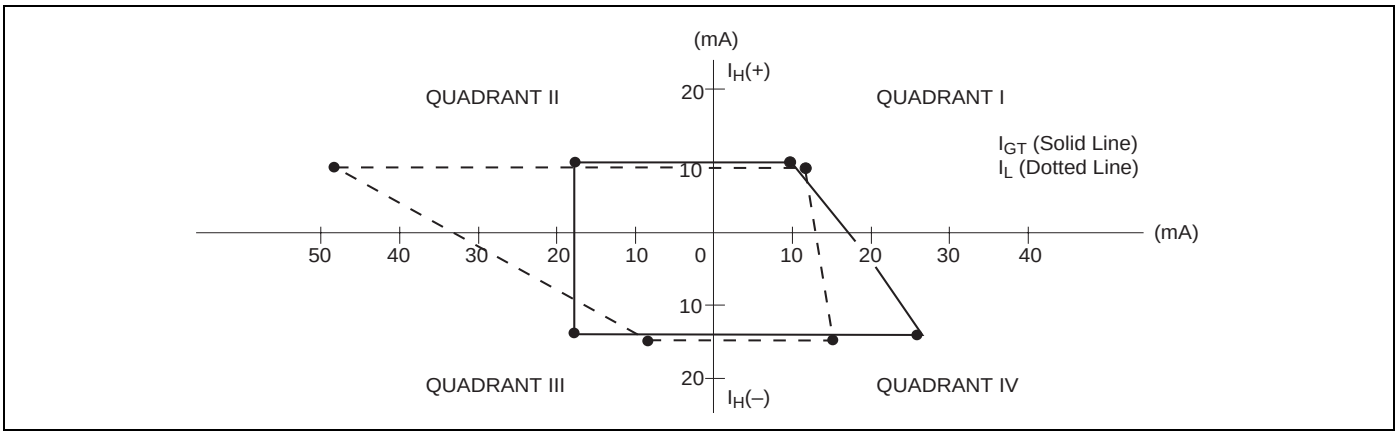


Figure AN1002.9 Typical Gating, Latching, and Holding Relationships of 4 A Triac at 25 °C

The relationships of gating, latching, and holding for several device types are shown in the following table. For convenience all ratios are referenced to Quadrant I gating.

Typical Ratio of Gating, Latching, and Holding Currents at 25 °C									
	Ratio								
Devices	$\frac{I_{GT(II)}}{I_{GT(I)}}$	$\frac{I_{GT(III)}}{I_{GT(I)}}$	$\frac{I_{GT(IV)}}{I_{GT(I)}}$	$\frac{I_{L(I)}}{I_{GT(I)}}$	$\frac{I_{L(II)}}{I_{GT(I)}}$	$\frac{I_{L(III)}}{I_{GT(I)}}$	$\frac{I_{L(IV)}}{I_{GT(I)}}$	$\frac{I_{H(+)}}{I_{GT(I)}}$	$\frac{I_{H(-)}}{I_{GT(I)}}$
4 A Triac	1.6	2.5	2.7	1.2	4.8	1.2	1.3	1.0	1.2
10 A Triac	1.5	1.4	3.1	1.6	4.0	1.8	2.0	1.1	1.6
15 A Alternistor	1.5	1.8	–	2.4	7.0	2.1	–	2.2	1.9
1 A Sensitive SCR	–	–	–	25	–	–	–	25	–
6 A SCR	–	–	–	3.2	–	–	–	2.6	–

Examples of a 10 A triac:

If $I_{GT}(I)$ = 10 mA, then
$I_{GT}(II)$ = 15 mA
$I_{GT}(III)$ = 14 mA
$I_{GT}(IV)$ = 31 mA

If $I_L(I)$ = 16 mA, then
$I_L(II)$ = 40 mA
$I_L(III)$ = 18 mA
$I_L(IV)$ = 20 mA

If $I_H(+)$ = 11 mA at 25 °C, then
$I_H(+)$ = 16 mA

Summary

Gating, latching, and holding current characteristics of thyristors are quite important yet predictable (once a single parameter value is known). Their interrelationships (ratios) can also be used to help designers in both initial circuit application design as well as device selection.

Notes

AN1003

Phase Control Using Thyristors

Introduction

Due to high-volume production techniques, thyristors are now priced so that almost any electrical product can benefit from electronic control. A look at the fundamentals of SCR and triac phase controls shows how this is possible.

Output Power Characteristics

Phase control is the most common form of thyristor power control. The thyristor is held in the off condition — that is, all current flow in the circuit is blocked by the thyristor except a minute leakage current. Then the thyristor is triggered into an “on” condition by the control circuitry.

For full-wave AC control, a single triac or two SCRs connected in inverse parallel may be used. One of two methods may be used for full-wave DC control — a bridge rectifier formed by two SCRs or an SCR placed in series with a diode bridge as shown in Figure AN1003.1.

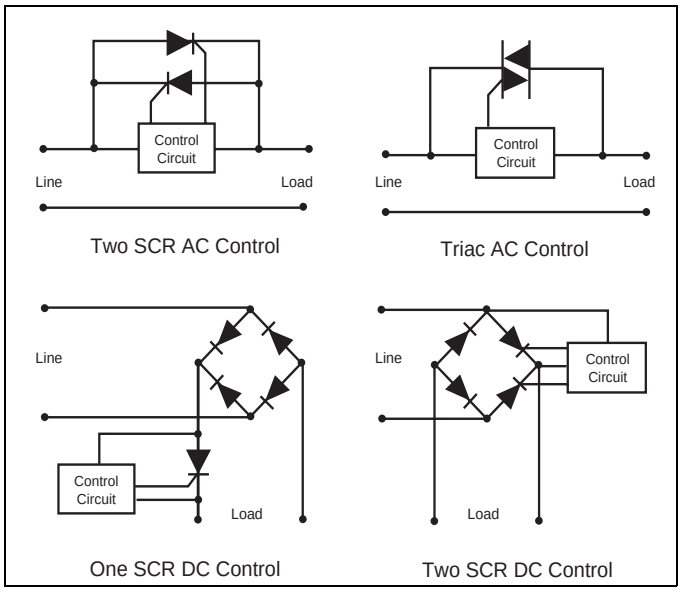


Figure AN1003.1 SCR/Triac Connections for Various Methods of Phase Control

Figure AN1003.2 illustrates voltage waveform and shows common terms used to describe thyristor operation. Delay angle is the time during which the thyristor blocks the line voltage. The conduction angle is the time during which the thyristor is on.

It is important to note that the circuit current is determined by the load and power source. For simplification, assume the load is resistive; that is, both the voltage and current waveforms are identical.

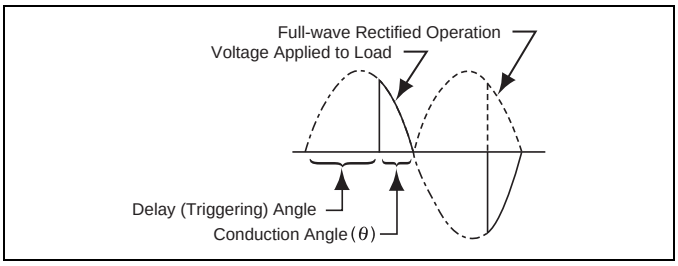


Figure AN1003.2 Sine Wave Showing Principles of Phase Control

Different loads respond to different characteristics of the AC waveform. For example, some are sensitive to average voltage, some to RMS voltage, and others to peak voltage. Various voltage characteristics are plotted against conduction angle for half- and full-wave phase control circuits in Figure AN1003.3 and Figure AN1003.4.

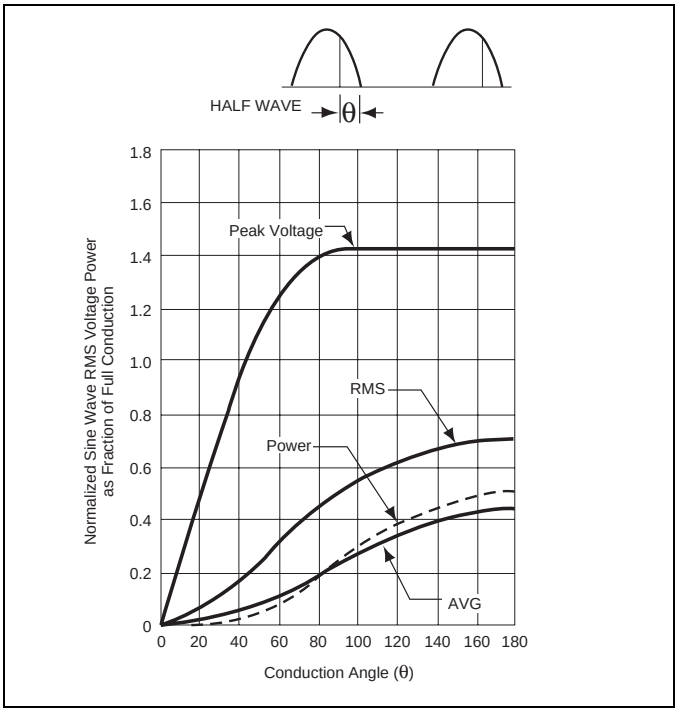


Figure AN1003.3 Half-Wave Phase Control (Sinusoidal)

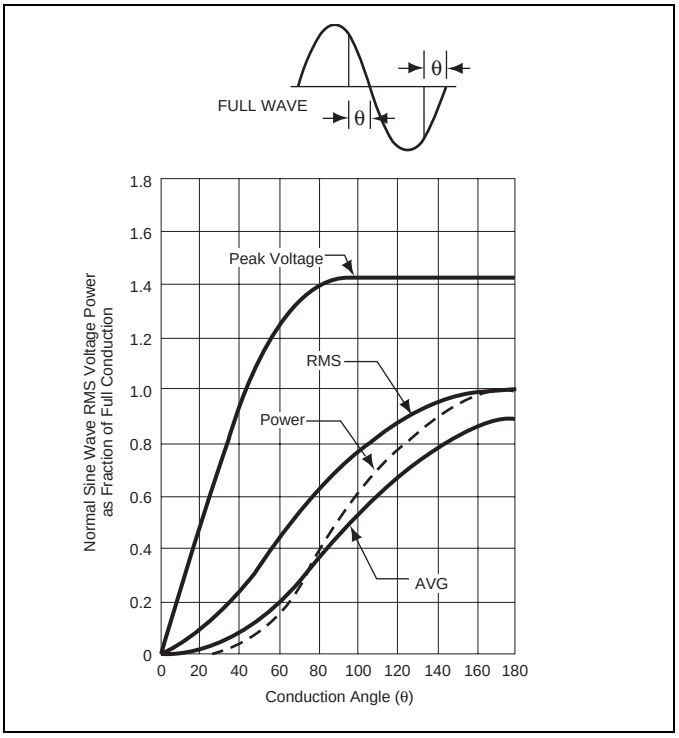


Figure AN1003.4 Symmetrical Full-Wave Phase Control (Sinusoidal)

Figure AN1003.3 and Figure AN1003.4 also show the relative power curve for constant impedance loads such as heaters. Because the relative impedance of incandescent lamps and motors change with applied voltage, they do not follow this curve precisely. To use the curves, find the full-wave rated power of the load, and then multiply by the ratio associated with the specific phase angle. Thus, a 180° conduction angle in a half-wave circuit provides 0.5 x full-wave conduction power.

In a full-wave circuit, a conduction angle of 150° provides 97% full power while a conduction angle of 30° provides only 3% of full power control. Therefore, it is usually pointless to obtain conduction angles less than 30° or greater than 150°.

Figure AN1003.5 and Figure AN1003.6 give convenient direct output voltage readings for 115 V/230 V input voltage. These curves also apply to current in a resistive circuit.

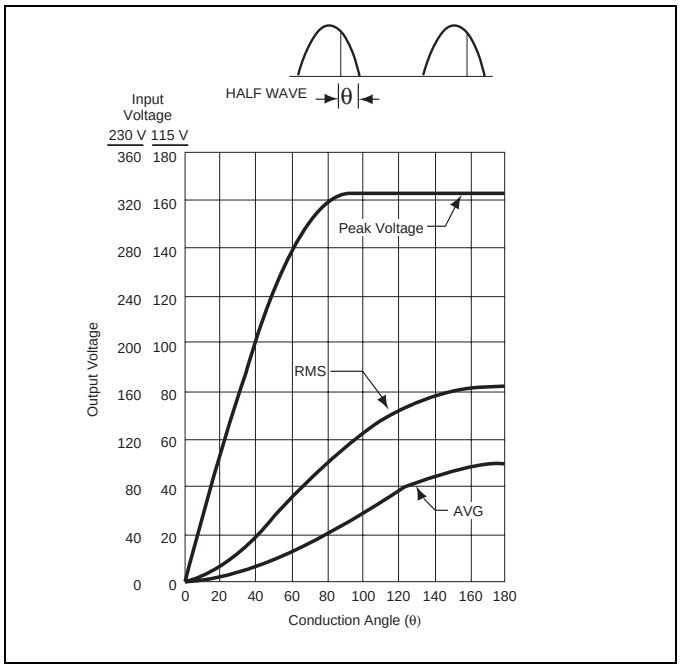


Figure AN1003.5 Output Voltage of Half-wave Phase

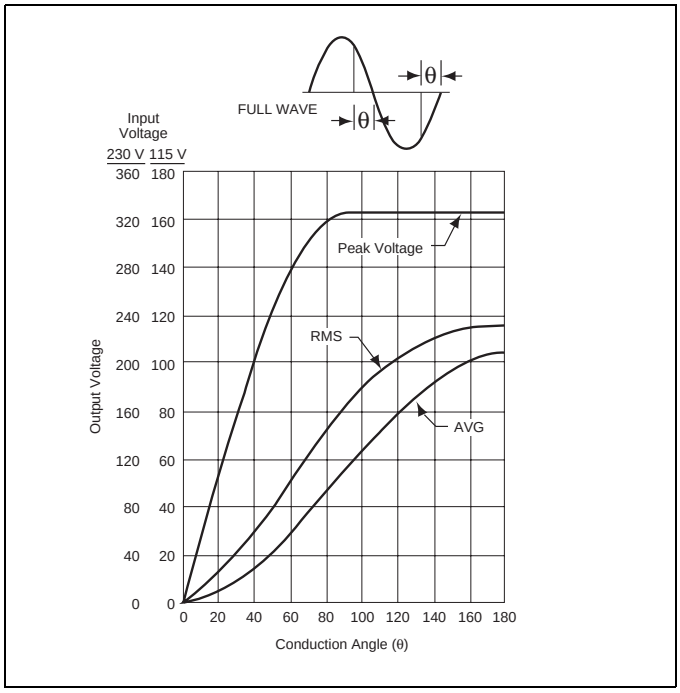


Figure AN1003.6 Output Voltage of Full-wave Phase Control

Control Characteristics

A relaxation oscillator is the simplest and most common control circuit for phase control. Figure AN1003.7 illustrates this circuit as it would be used with a thyristor. Turn-on of the thyristor occurs when the capacitor is charged through the resistor from a voltage or current source until the breakover voltage of the switching device is reached. Then, the switching device changes to its on state, and the capacitor is discharged through the thyristor gate. Trigger devices used are neon bulbs, unijunction transistors, and three-, four-, or five-layer semiconductor trigger devices. Phase control of the output waveform is obtained by varying the RC time constant of the charging circuit so the trigger device breakdown occurs at different phase angles within the controlled half or full cycle.

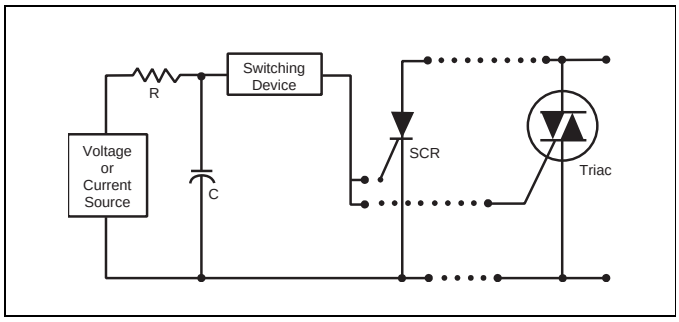


Figure AN1003.7 Relaxation Oscillator Thyristor Trigger Circuit

Figure AN1003.8 shows the capacitor voltage-time characteristic if the relaxation oscillator is to be operated from a pure DC source.

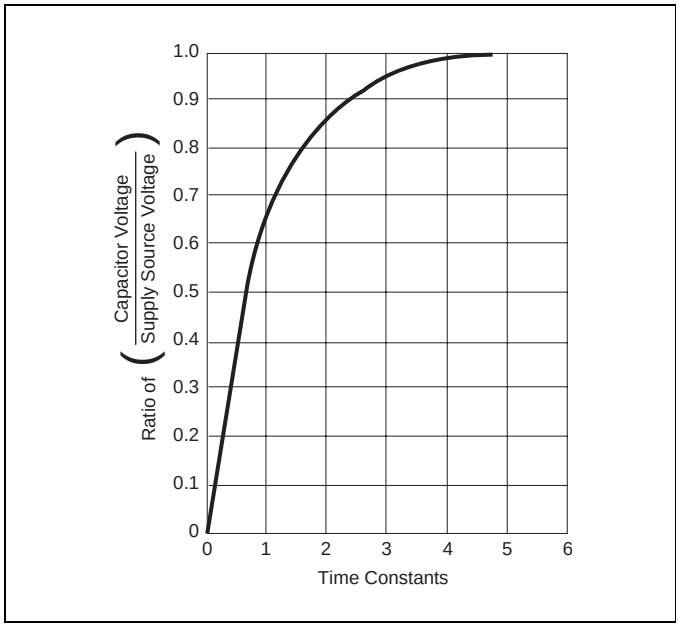


Figure AN1003.8 Capacitor Charging from DC Source

Usually, the design starting point is the selection of a capacitance value which will reliably trigger the thyristor when the capacitance is discharged. Trigger devices and thyristor gate triggering characteristics play a part in the selection. All the device characteristics are not always completely specified in applications, so experimental determination is sometimes needed.

Upon final selection of the capacitor, the curve shown in Figure AN1003.8 can be used in determining the charging resistance needed to obtain the desired control characteristics.

Many circuits begin each half-cycle with the capacitor voltage at or near zero. However, most circuits leave a relatively large residual voltage on the capacitor after discharge. Therefore, the charging resistor must be determined on the basis of additional charge necessary to raise the capacitor to trigger potential.

For example, assume that we want to trigger an S2010L SCR with a 32 V trigger diac. A 0.1 µF capacitor will supply the necessary SCR gate current with the trigger diac. Assume a 50 V dc power supply, 30° minimum conduction angle, and 150° maximum conduction angle with a 60 Hz input power source. At approximately 32 V, the diac triggers leaving 0.66 V_{BO} of diac voltage on the capacitor. In order for diac to trigger, 22 V must be added to the capacitor potential, and 40 V additional (50-10) are available. The capacitor must be charged to 22/40 or 0.55 of the available charging voltage in the desired time. Looking at Figure AN1003.8, 0.55 of charging voltage represents 0.8 time constant. The 30° conduction angle required that the firing pulse be delayed 150° or 6.92 ms. (The period of 1/2 cycle at 60 Hz is 8.33 ms.) To obtain this time delay:

6.92 ms = 0.8 RC
RC = 8.68 ms

if C = 0.10 µF

then, $R = \frac{8.68\times10^{-3}}{0.1\times10^{-6}} = 86{,}000\ \Omega$

To obtain the minimum R (150° conduction angle), the delay is 30° or

(30/180) x 8.33 = 1.39 ms
1.39 ms = 0.8 RC
RC = 1.74 ms

$R = \frac{1.74\times10^{-3}}{0.1\times10^{-6}} = 17{,}400\ \Omega$

Using practical values, a 100 k potentiometer with up to 17 k minimum (residual) resistance should be used. Similar calculations using conduction angles between the maximum and minimum values will give control resistance versus power characteristic of this circuit.

Triac Phase Control

The basic full-wave triac phase control circuit shown in Figure AN1003.9 requires only four components. Adjustable resistor R_1 and C_1 are a single-element phase-shift network. When the voltage across C_1 reaches breakover voltage (V_{BO}) of the diac, C_1 is partially discharged by the diac into the triac gate. The triac is then triggered into the conduction mode for the remainder of that half-cycle. In this circuit, triggering is in Quadrants I and III. The unique simplicity of this circuit makes it suitable for applications with small control range.

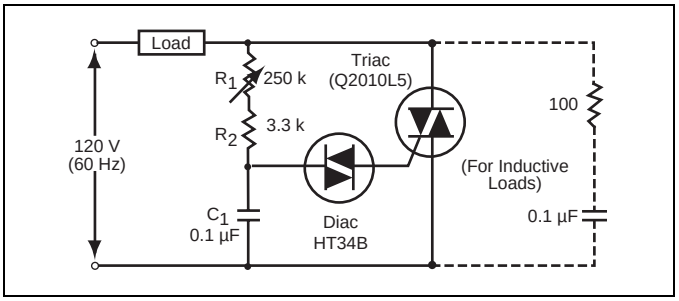


Figure AN1003.9 Basic Diac-Triac Phase Control

The hysteresis (snap back) effect is somewhat similar to the action of a kerosene lantern. That is, when the control knob is first rotated from the off condition, the lamp can be lit only at some intermediate level of brightness, similar to turning up the wick to light the lantern. Brightness can then be turned down until it finally reaches the extinguishing point. If this occurs, the lamp can only be relit by turning up the control knob again to the intermediate level. Figure AN1003.10 illustrates the hysteresis effect in capacitor-diac triggering. As R_1 is brought down from its maximum resistance, the voltage across the capacitor increases until the diac first fires at point A, at the end of a half-cycle (conduction angle θi). After the gate pulse, however, the capacitor voltage drops suddenly to about half the triggering voltage, giving the capacitor a different initial condition. The capacitor charges to the diac, triggering voltage at point B in the next half-cycle and giving a steady-state conduction angle shown as θ for the triac.

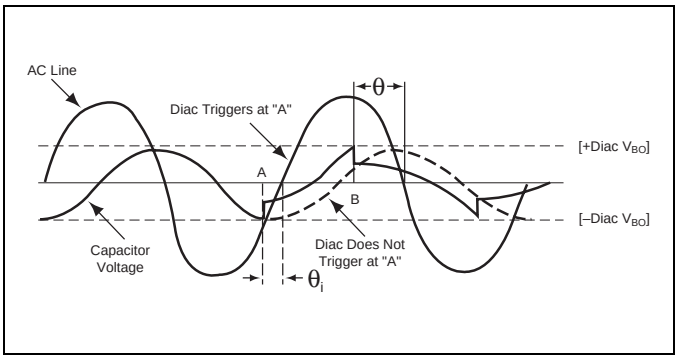


Figure AN1003.10 Relationship of AC Line Voltage and Triggering Voltage

In the Figure AN1003.11 illustration, the addition of a second RC phase-shift network extends the range on control and reduces the hysteresis effect to a negligible region. This circuit will control from 5% to 95% of full load power, but is subject to supply voltage variations. When R_1 is large, C_1 is charged primarily through R_3 from the phase-shifted voltage appearing across C_2. This action provides additional range of phase-shift across C_1 and enables C_2 to partially recharge C_1 after the diac has triggered, thus reducing hysteresis. R_3 should be adjusted so that the circuit just drops out of conduction when R_1 is brought to maximum resistance.

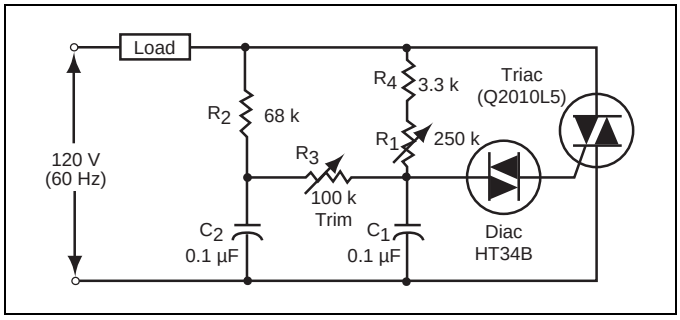


Figure AN1003.11 Extended Range Full-wave Phase Control

By using one of the circuits shown in Figure AN1003.12, the hysteresis effect can be eliminated entirely. The circuit (a) resets the timing capacitor to the same level after each positive half-cycle, providing a uniform initial condition for the timing capacitor. This circuit is useful only for resistive loads since the firing angle is not symmetrical throughout the range. If symmetrical firing is required, use the circuit (b) shown in Figure AN1003.12.

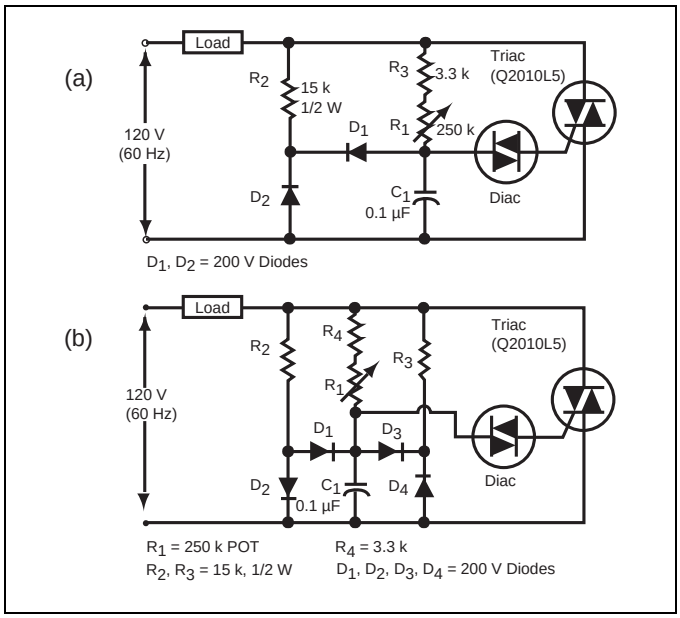
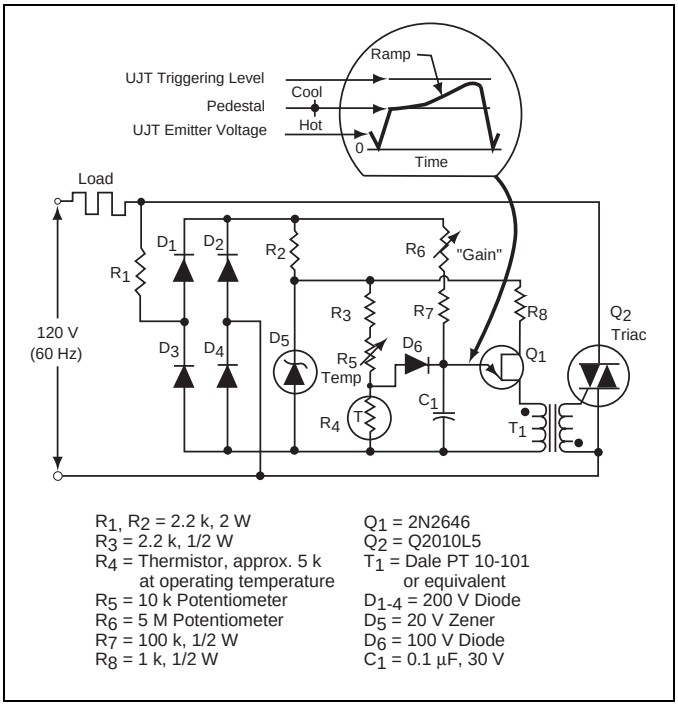


Figure AN1003.12 Wide-range Hysteresis Free Phase Control

For more complex control functions, particularly closed loop controls, the unijunction transistor may be used for the triggering device in a ramp and pedestal type of firing circuit as shown in Figure AN1003.13.

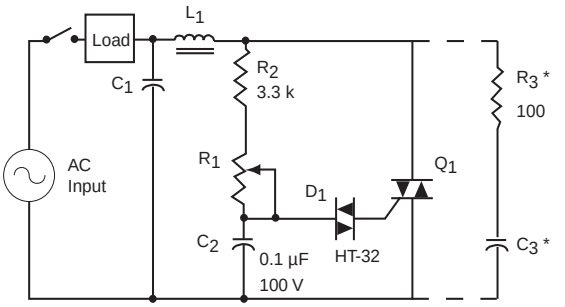


R_1, R_2 = 2.2 k, 2 W
R_3 = 2.2 k, 1/2 W
R_4 = Thermistor, approx. 5 k at operating temperature
R_5 = 10 k Potentiometer
R_6 = 5 M Potentiometer
R_7 = 100 k, 1/2 W
R_8 = 1 k, 1/2 W
Q_1 = 2N2646
Q_2 = Q2010L5
T_1 = Dale PT 10-101 or equivalent
D_{1-4} = 200 V Diode
D_5 = 20 V Zener
D_6 = 100 V Diode
C_1 = 0.1 µF, 30 V

Figure AN1003.13 Precision Proportional Temperature Control

Several speed control and light dimming (phase) control circuits have been presented that give details for a complete 120 V application circuit but none for 240 V. Figure AN1003.14 and Figure AN1003.15 show some standard phase control circuits for 240 V, 60 Hz/50 Hz operation along with 120 V values for comparison. Even though there is very little difference, there are a few key things that must be remembered. First, capacitors and triacs connected across the 240 V line must be rated at 400 V. Secondly, the potentiometer (variable resistor) value must change considerably to obtain the proper timing or triggering for 180° in each half-cycle.

Figure AN1003.14 shows a simple single-time-constant light dimmer (phase control) circuit, giving values for both 120 V and 240 V operation.



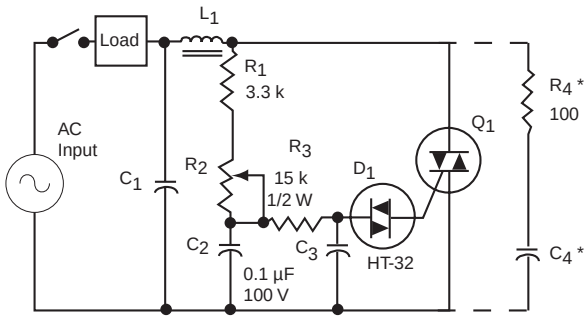
Note: L_1 and C_1 form an RFI filter that may be eliminated

* dv/dt snubber network when required

AC Input Voltage	AC Load Current	R_1	C_1, C_3	L_1	Q_1
120 V ac 60 Hz	12 A	250 k	0.1 µF 200 V	100 µH	Q2016LH6
240 V ac 50/60 Hz	3 A	500 k	0.1 µF 400 V	200 µH	Q4004L4

Figure AN1003.14 Single-time-constant Circuit for Incandescent Light Dimming, Heat Control, and Motor Speed Control

The circuit shown in Figure AN1003.15 is a double-time-constant circuit which has improved performance compared to the circuit shown in Figure AN1003.14. This circuit uses an additional RC network to extend the phase angle so that the triac can be triggered at small conduction angles. The additional RC network also minimizes any hysteresis effect explained and illustrated in Figure AN1003.10 and Figure AN1003.11.



Note: L_1 and C_1 form an RFI filter that may be eliminated

* dv/dt snubber network when required

AC Input Voltage	AC Load Current	R_2	C_1, C_2, C_4	L_1	Q_1
120 V ac 60 Hz	8 A	250 k	0.1 µF 200 V	100 µH	Q2010LH5
240 V ac 50 Hz	6 A	500 k	0.1 µF 400 V	200 µH	Q4008LH4
240 V ac 60 Hz	6 A	500 k	0.1 µF 400 V	200 µH	Q4008LH4

Figure AN1003.15 Double-time-constant Circuit for Incandescent Light Dimming, Heat Control, and Motor Speed Control

Permanent Magnet Motor Control

Figure AN1003.16 illustrates a circuit for phase controlling a permanent magnet (PM) motor. Since PM motors are also generators, they have characteristics that make them difficult for a standard triac to commutate properly. Control of a PM motor is easily accomplished by using an alternistor triac with enhanced commutating characteristics.

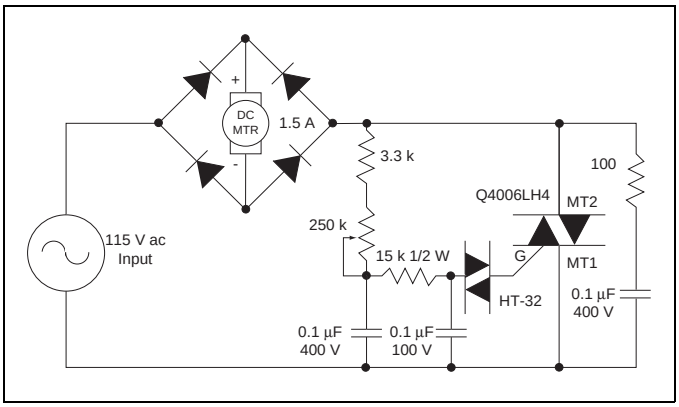
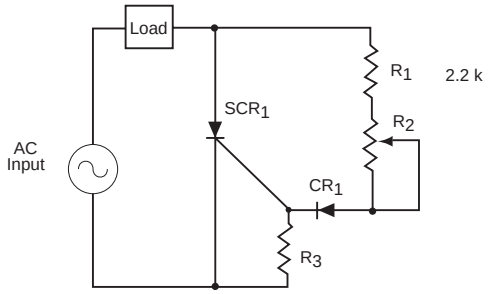


Figure AN1003.16 Circuit for Phase Controlling a Permanent Magnet Motor

PM motors normally require full-wave DC rectification. Therefore, the alternistor triac controller should be connected in series with the AC input side of the rectifier bridge. The possible alternative of putting an SCR controller in series with the motor on the DC side of the rectifier bridge can be a challenge when it comes to timing and delayed turn-on near the end of the half cycle. The alternistor triac controller shown in Figure AN1003.16 offers a wide range control so that the alternistror triac can be triggered at a small conduction angle or low motor speed; the rectifiers and alternistors should have similar voltage ratings, with all based on line voltage and actual motor load requirements.

SCR Phase Control

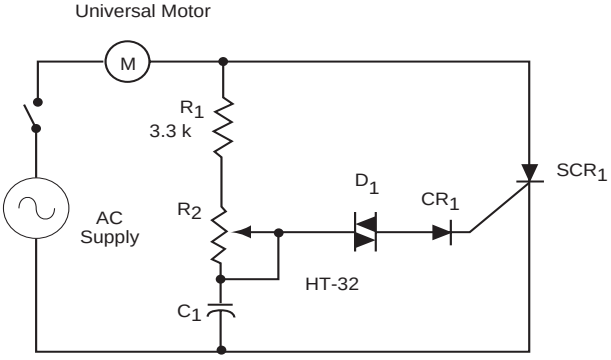
Figure AN1003.17 shows a very simple variable resistance half-wave circuit. It provides phase retard from essentially zero (SCR full on) to 90 electrical degrees of the anode voltage wave (SCR half on). Diode CR_1 blocks reverse gate voltage on the negative half-cycle of anode supply voltage. This protects the reverse gate junction of sensitive SCRs and keeps power dissipation low for gate resistors on the negative half cycle. The diode is rated to block at least the peak value of the AC supply voltage. The retard angle cannot be extended beyond the 90-degree point because the trigger circuit supply voltage and the trigger voltage producing the gate current to fire are in phase. At the peak of the AC supply voltage, the SCR can still be triggered with the maximum value of resistance between anode and gate. Since the SCR will trigger and latch into conduction the first time I_{GT} is reached, its conduction cannot be delayed beyond 90 electrical degrees with this circuit.



AC Input Voltage	AC Load Current	R_2	CR_1	SCR_1	R_3
120 V ac 60 Hz	0.8 A	500 k	IN4003	EC103B	1 k
120 V ac 60 Hz	8.5 A	100 k	IN4003	S2010F1	Not Required
240 V ac 60 Hz	0.8 A	1 M	IN4004	EC103D	1 k
240 V ac 60 Hz	8.5 A	250 k	IN4004	S4010F1	Not Required
240 V ac 50Hz	2.5 A	1 M	IN4004	T106D1	1 k

Figure AN1003.17 Half-wave Control, 0° to 90° Conduction

Figure AN1003.18 shows a half-wave phase control circuit using an SCR to control a universal motor. This circuit is better than simple resistance firing circuits because the phase-shifting characteristics of the RC network permit the firing of the SCR beyond the peak of the impressed voltage, resulting in small conduction angles and very slow speed.



AC Input Voltage	AC Load Current	R_2	CR_1	SCR_1	C_1
120 V ac 60 Hz	8 A	150 k	IN4003	S2015L	0.1µF 200 V
240 V ac 60 Hz	6.5 A	200 k	IN4004	S4008L	0.1µF 400 V
240 V ac 50 Hz	6.5 A	200 k	IN4004	S4008L	0.1µF 400 V

Figure AN1003.18 Half-wave Motor Control

Phase Control from Logic (DC) Inputs

Triacs can also be phase-controlled from pulsed DC unidirectional inputs such as those produced by a digital logic control system. Therefore, a microprocessor can be interfaced to AC load by using a sensitive gate triac to control a lamp's intensity or a motor's speed.

There are two ways to interface the unidirectional logic pulse to control a triac. Figure AN1003.19 illustrates one easy way if load current is approximately 5 A or less. The sensitive gate triac serves as a direct power switch controlled by HTL, TTL, CMOS, or integrated circuit operational amplifier. A timed pulse from the system's logic can activate the triac anywhere in the AC sine-wave producing a phase-controlled load.

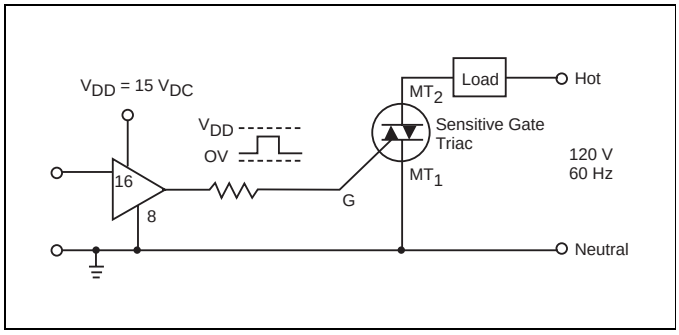


Figure AN1003.19 Sensitive Gate Triac Operating in Quadrants I and IV

The key to DC pulse control is correct grounding for DC and AC supply. As shown in Figure AN1003.19, **DC ground and AC ground/neutral must be common** plus **MT1 must be connected to common ground**. MT1 of the triac is the return for both main terminal junctions as well as the gate junction.

Figure AN1003.20 shows an example of a unidirectional (all negative) pulse furnished from a special I.C. that is available from LSI Computer Systems in Melville, New York. Even though the circuit and load is shown to control a Halogen lamp, it could be applied to a common incandescent lamp for touch-controlled dimming.

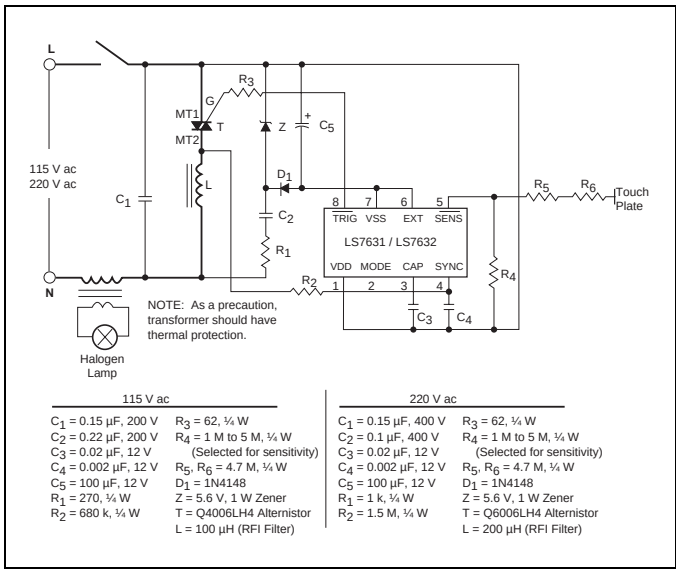


Figure AN1003.20 Typical Touch Plate Halogen Lamp Dimmer

For a circuit to control a heavy-duty inductive load where an alternistor is not compatible or available, two SCRs can be driven by an inexpensive TO-92 triac to make a very high current triac or alternistor equivalent, as shown in Figure AN1003.21. See "Relationship of IAV, IRMS, and IPK' in AN1009 for design calculations.

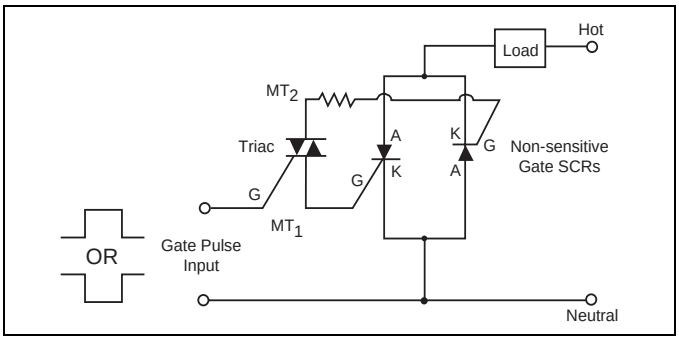


Figure AN1003.21 Triac Driving Two Inverse Parallel Non-Sensitive Gate SCRs

Figure AN1003.22 shows another way to interface a unidirectional pulse signal and activate AC loads at various points in the AC sine wave. This circuit has an electrically-isolated input which allows load placement to be flexible with respect to AC line. In other words, connection between DC ground and AC neutral is not required.

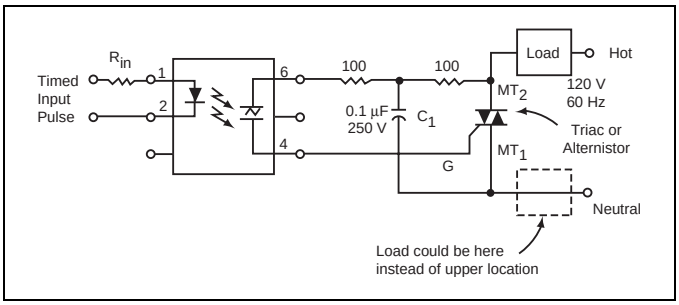


Figure AN1003.22 Opto-isolator Driving a Triac or Alternistor

Microcontroller Phase Control

Traditionally, microcontrollers were too large and expensive to be used in small consumer applications such as a light dimmer. Microchip Technology Inc. of Chandler, Arizona has developed a line of 8-pin microcontrollers without sacrificing the functionality of their larger counterparts. These devices do not provide high drive outputs, but when combined with a sensitive triac can be used in a cost-effective light dimmer.

Figure AN1003.23 illustrates a simple circuit using a transformerless power supply, PIC 12C508 microcontroller, and a sensitive triac configured to provide a light dimmer control. R_3 is connected to the hot lead of the AC power line and to pin GP_4. The ESD protection diodes of the input structure allow this connection without damage. When the voltage on the AC power line is positive, the protection diode form the input to V_{DD} is forward biased, and the input buffer will see approximately V_{DD} + 0.7 V. The software will read this pin as high. When the voltage on the line is negative, the protection diode from V_{SS} to the input pin is forward biased, and the input buffer sees approximately V_{SS} - 0.7 V. The software will read the pin as low. By polling GP_4 for a change in state, the software can detect zero crossing.

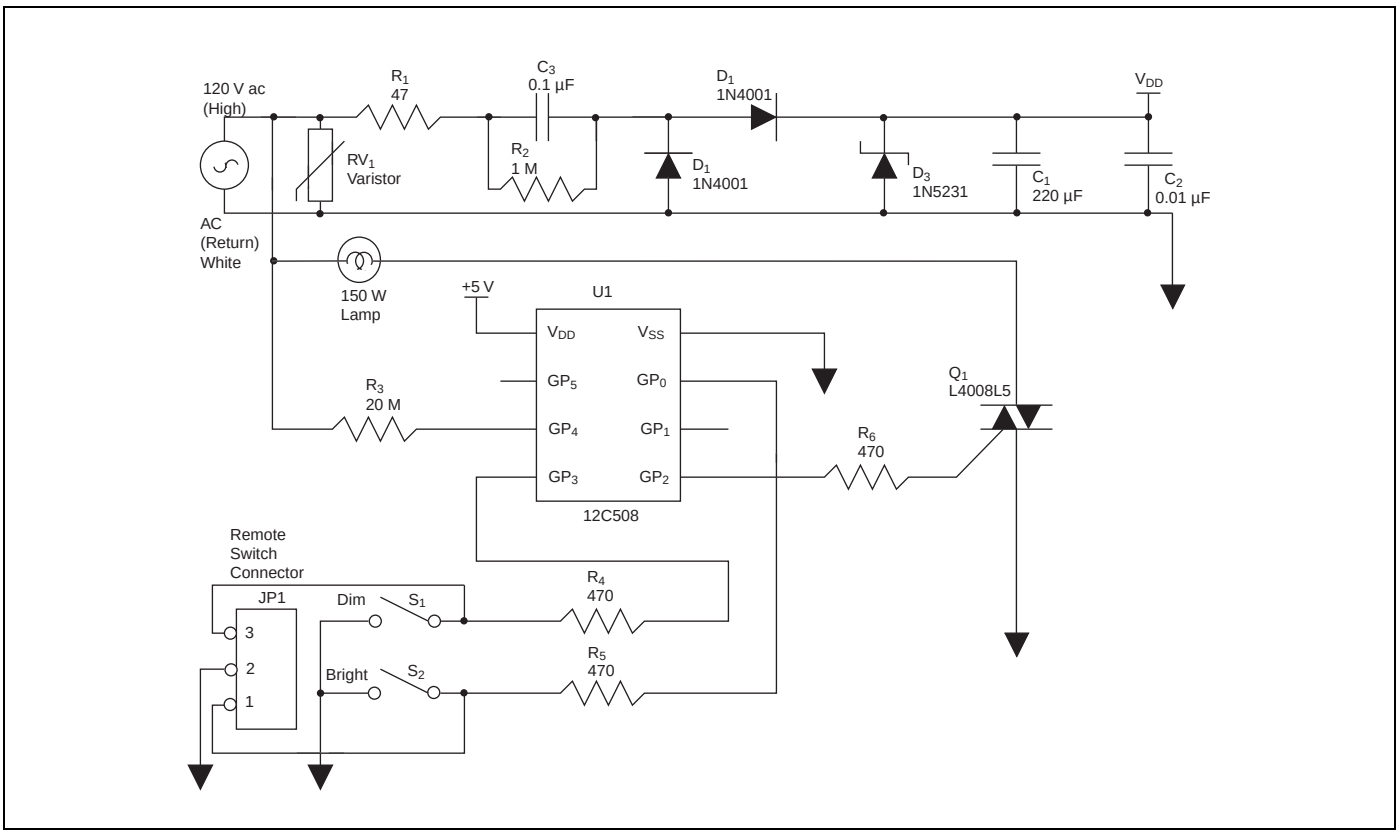


Figure AN1003.23 Microcontroller Light Dimmer Control

With a zero crossing state detected, software can be written to turn on the triac by going from tri-state to a logic high on the gate and be synchronized with the AC phase cycles (Quadrants I and IV). Using pull-down switches connected to the microcontoller inputs, the user can signal the software to adjust the duty cycle of the triac.

For higher amperage loads, a small 0.8 A, TO-92 triac (operating in Quadrants I and IV) can be used to drive a 25 A alternistor triac (operating in Quadrants I and III) as shown in the heater control illustration in Figure AN1003.24.

For a complete listing of the software used to control this circuit, see the Microchip application note PICREF-4. This application note can be downloaded from Microchip's Web site at www.microchip.com.

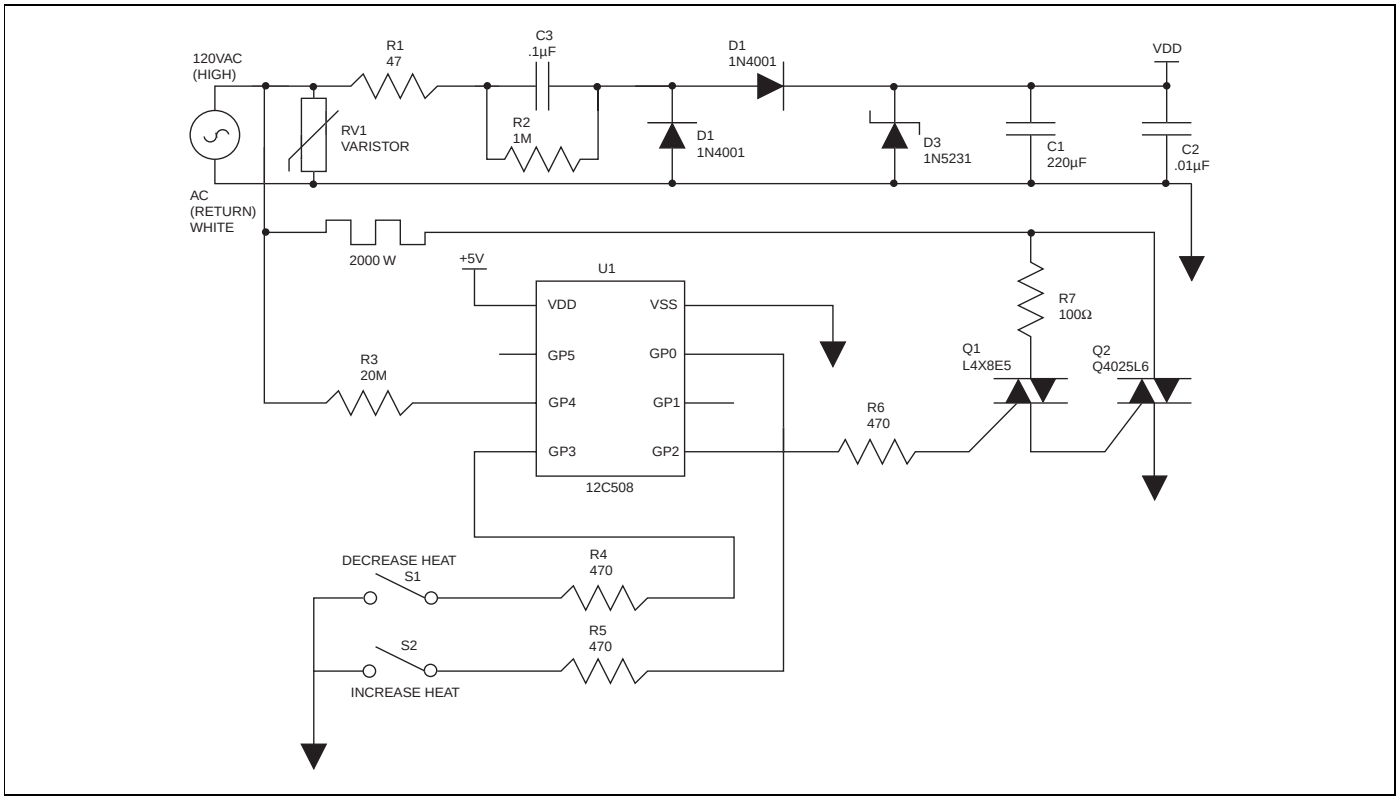


Figure AN1003.24 Microcontroller Heater Control

Summary

The load currents chosen for the examples in this application note were strictly arbitrary, and the component values will be the same regardless of load current except for the power triac or SCR. The voltage rating of the power thyristor devices must be a minimum of 200 V for 120 V input voltage and 400 V for 240 V input voltage.

The use of alternistors instead of triacs may be much more acceptable in higher current applications and may eliminate the need for any dv/dt snubber network.

For many electrical products in the consumer market, competitive thyristor prices and simplified circuits make automatic control a possibility. These simple circuits give the designer a good feel for the nature of thyristor circuits and their design. More sophistication, such as speed and temperature feedback, can be developed as the control techniques become more familiar. A remarkable phenomenon is the degree of control obtainable with very simple circuits using thyristors. As a result, industrial and consumer products will greatly benefit both in usability and marketability.

Notes

AN1004

Mounting and Handling of Semiconductor Devices

Introduction

Proper mounting and handling of semiconductor devices, particularly those used in power applications, is an important, yet sometimes overlooked, consideration in the assembly of electronic systems. Power devices need adequate heat dissipation to increase operating life and reliability and allow the device to operate within manufacturers' specifications. Also, in order to avoid damage to the semiconductor chip or internal assembly, the devices should not be abused during assembly. Very often, device failures can be attributed directly to a heat sinking or assembly damage problem.

The information in this application note guides the semiconductor user in the proper use of Teccor devices, particularly the popular and versatile TO-220 and TO-202 epoxy packages.

Contact the Teccor Applications Engineering Group for further details or suggestions on use of Teccor devices.

Lead Forming — Typical Configurations

A variety of mounting configurations are possible with Teccor power semiconductor TO-202, TO-92, DO-15X, and TO-220 packages, depending upon such factors as power requirements, heat sinking, available space, and cost considerations. Figure AN1004.1 shows typical examples and basic design rules.

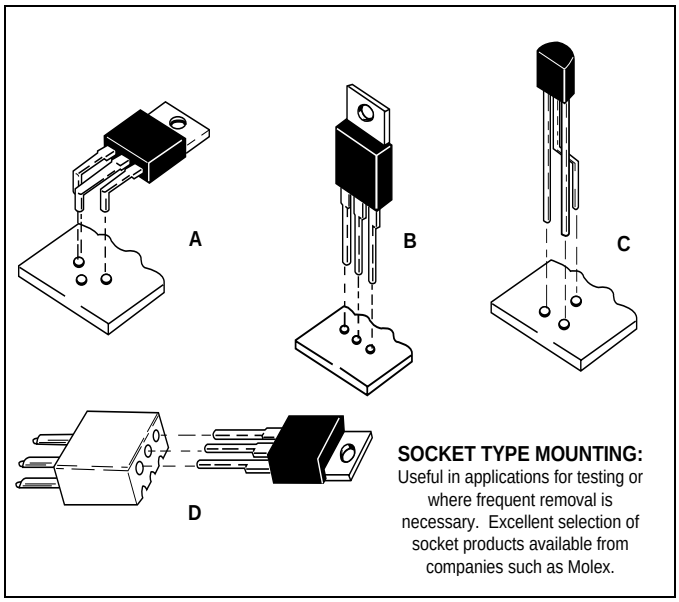


Figure AN1004.1 Component Mounting

These are suitable only for vibration-free environments and low-power, free-air applications. For best results, the device should be in a vertical position for maximum heat dissipation from convection currents.

Standard Lead Forms

Teccor encourages users to allow factory production of all lead and tab form options. Teccor has the automated machinery and expertise to produce pre-formed parts at minimum risk to the device and with greater convenience for the consumer. See the “Lead Form Dimensions” section of this catalog for a complete list of readily available lead form options. Contact Teccor for information regarding custom lead form designs.

Lead Bending Method

Leads may be bent easily and to any desired angle, provided that the bend is made at a minimum 0.063" (0.1" for TO-218 package) away from the package body with a minimum radius of 0.032" (0.040" for TO-218 package) or 1.5 times lead thickness rule. DO-15X device leads may be bent with a minimum radius of 0.050”, and DO-35 device leads may be bent with a minimum radius of 0.028”. Leads should be held firmly between the package body and the bend so that strain on the leads is not transmitted to the package body, as shown in Figure AN1004.2. Also, leads should be held firmly when trimming length.

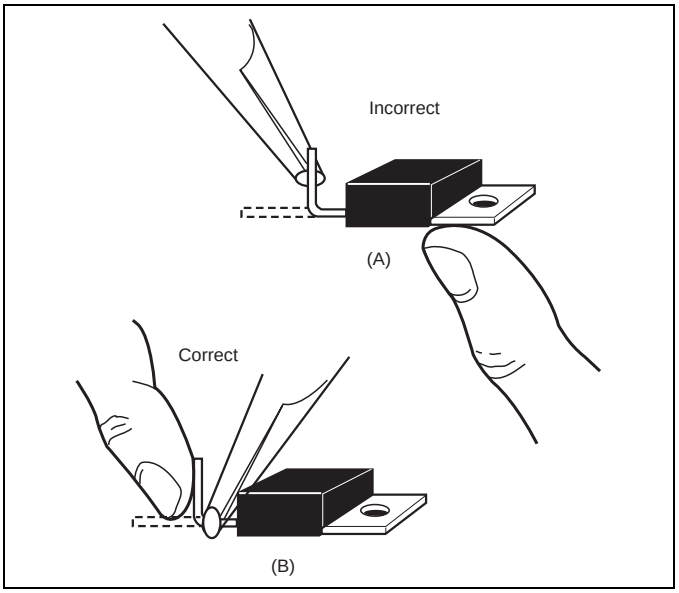


Figure AN1004.2 Lead Bending Method

When bending leads in the plane of the leads (spreading), bend only the narrow part. Sharp angle bends should be done only once as repetitive bending will fatigue and break the leads.

The mounting tab of the TO-202 package may also be bent or formed into any convenient shape as long as it is held firmly between the plastic case and the area to be formed or bent. Without this precaution, bending the tab may fracture the chip and permanently damage the unit.

Heat Sinking

Use of the largest, most efficient heat sink as is practical and cost effective extends device life and increases reliability. In the illustration shown in Figure AN1004.3, each device is electrically isolated.

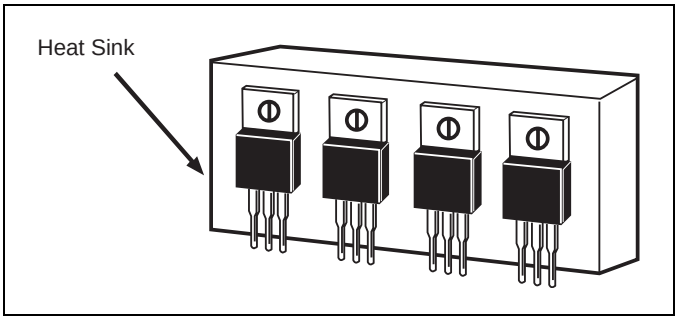


Figure AN1004.3 Several Isolated TO-220 Devices Mounted to a Common Heat Sink

Many power device failures are a direct result of improper heat dissipation. Heat sinks with a mating area smaller than the metal tab of the device are unacceptable. Heat sinking material should be at least 0.062" thick to be effective and efficient.

Note that in all applications the maximum case temperature (T_C) rating of the device must not be exceeded. Refer to the individual device data sheet rating curves (T_C versus I_T) as well as the individual device outline drawings for correct T_C measurement point.

Figure AN1004.4 through Figure AN1004.6 show additional examples of acceptable heat sinks.

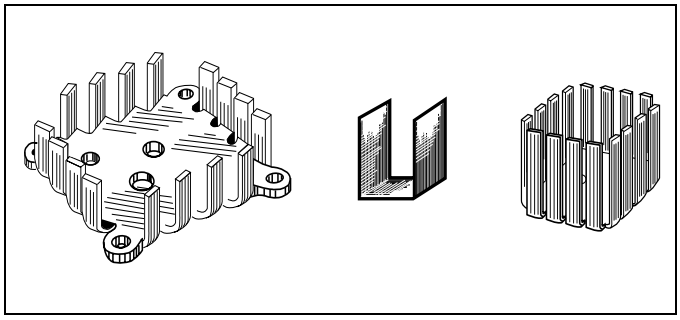


Figure AN1004.4 Examples of PC Board Mounts

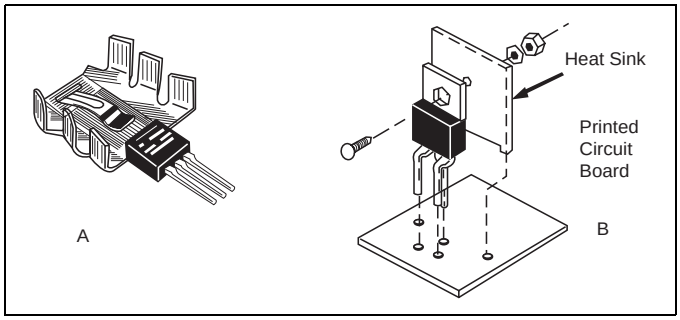


Figure AN1004.5 Vertical Mount Heat Sink

Several types of vertical mount heat sinks are available. Keep heat sink vertical for maximum convection.

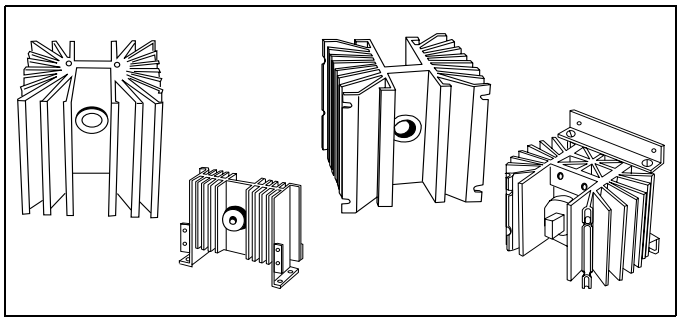


Figure AN1004.6 Examples of Extruded Aluminum

When coupled with fans, extruded aluminum mounts have the highest efficiency.

Heat Sinking Notes

Care should be taken not to mount heat sinks near other heat-producing elements such as power resistors, because black anodized heat sinks may absorb more heat than they dissipate.

Some heat sinks can hold several power devices. Make sure that if they are in electrical contact to the heat sink, the devices do not short-circuit the desired functions. Isolate the devices electrically or move to another location. Recall that the mounting tab of Teccor isolated TO-220 devices is electrically isolated so that several devices may be mounted on the same heat sink without extra insulating components. If using an external insulator such as mica, with a thickness of 0.004", an additional thermal resistance of 0.8° C/W for TO-220 or 0.5° C/W for TO-218 devices is added to the $R_{\theta JC}$ device rating.

Allow for adequate ventilation. If possible, route heat sinks to outside of assembly for maximum airflow.

Mounting Surface Selection

Proper mounting surface selection is essential to efficient transfer of heat from the semiconductor device to the heat sink and from the heat sink to the ambient. The most popular heat sinks are flat aluminum plates or finned extruded aluminum heat sinks.

The mounting surface should be clean and free from burrs or scratches. It should be flat within 0.002 inch per inch, and a surface finish of 30 to 60 microinches is acceptable. Surfaces with a higher degree of polish do not produce better thermal conductivity.

Many aluminum heat sinks are black anodized to improve thermal emissivity and prevent corrosion. Anodizing results in high electrical but negligible thermal insulation. This is an excellent choice for isolated TO-220 devices. For applications of TO-202 devices where electrical connection to the common anode tab is required, the anodization should be removed. Iridite or chromate acid dip finish offers low electrical and thermal resistance. Either TO-202 or isolated TO-220 devices may be mounted directly to this surface, regardless of application. Both finishes should be cleaned prior to use to remove manufacturing oils and films. Some of the more economical heat sinks are painted black. Due to the high thermal resistance of paint, the paint should be removed in the area where the semiconductor is attached.

Bare aluminum should be buffed with #000 steel wool and followed with an acetone or alcohol rinse. Immediately, thermal grease should be applied to the surface and the device mounted down to prevent dust or metal particles from lodging in the critical interface area.

For good thermal contact, the use of thermal grease is essential to fill the air pockets between the semiconductor and the mounting surface. This decreases the thermal resistance by 20%. For example, a typical TO-220 with $R_{\theta JC}$ of 1.2 °C/W may be lowered to 1 °C/W by using thermal grease.

Teccor recommends Dow-Corning 340 as a proven effective thermal grease. Fibrous applicators are not recommended as they may tend to leave lint or dust in the interface area. Ensure that the grease is spread adequately across the device mounting surface, and torque down the device to specification.

Contact Teccor Applications Engineering for assistance in choosing and using the proper heat sink for specific application.

Hardware And Methods

TO-220

The mounting hole for the Teccor TO-220 devices should not exceed 0.140” (6/32) clearance. (Figure AN1004.7) No insulating bushings are needed for the L Package (isolated) devices as the tab is electrically isolated from the semiconductor chip. 6/32 mounting hardware, especially round head or Fillister machine screws, is recommended and should be torqued to a value of 6 inch-lbs.

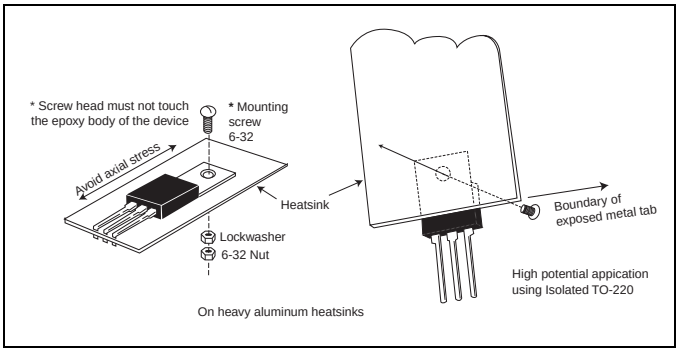


Figure AN1004.7 TO-220 Mounting

Punched holes are not acceptable due to cratering around the hole which can cause the device to be pulled into the crater by the fastener or can leave a significant portion of the device out of contact with the heat sink. The first effect may cause immediate damage to the package and early failure, while the second can create higher operating temperatures which will shorten operating life. Punched holes are quite acceptable in thin metal plates where fine-edge blanking or sheared-through holes are employed.

Drilled holes must have a properly prepared surface. Excessive chamfering is not acceptable as it may create a crater effect. Edges must be deburred to promote good contact and avoid puncturing isolation materials.

For high-voltage applications, it is recommended that only the metal portion of the TO-220 package (as viewed from the bottom of the package) be in contact with the heat sink. This will provide maximum oversurface distance and prevent a high voltage path over the plastic case to a grounded heat sink.

TO-202

The mounting hole for the Teccor TO-202 devices should not exceed 0.112” (4/40) clearance. (Figure AN1004.8) Since tab is electrically common with anode, heat sink may or may not need to be electrically isolated from tab. If not, use 4/40 screw with lock washer and nut. Mounting torque is 6 inch-lbs.

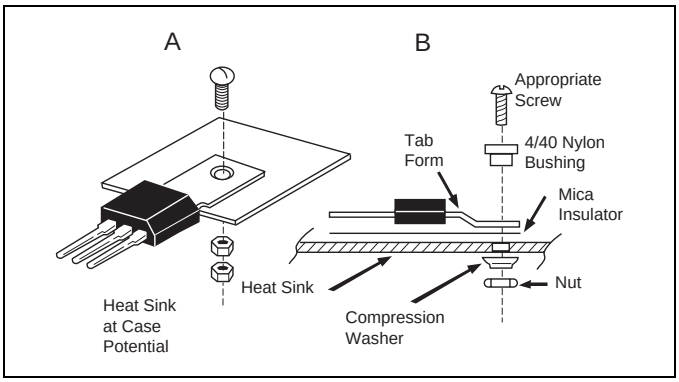


Figure AN1004.8 TO-202 Mounting

A nylon bushing and mica insulation are required to insulate the tab in an isolated application. A compression washer is recommended to avoid damage to the bushing. Do not attempt to mount non-formed tabs to a plane surface, as the resulting strain on the case may cause it or the semiconductor chip assembly to fail. Teccor has the facilities and expertise to properly tab form TO-202 devices for the convenience of the consumer.

TO-218

The mounting hole for the TO-218 device should not exceed 0.164” (8/32) clearance. Isolated versions of TO-218 do not require any insulating material since mounting tab is electrically isolated from the semiconductor chip. Round lead or Fillister machine screws are recommended. Maximum torque to be applied to mounting tab should not exceed 8 inch-lbs.

The same precautions given for the TO-220 package concerning punched holes, drilled holes, and proper prepared heat sink mounting surface apply to the TO-218 package. Also for high-voltage applications, it is recommended that only the metal portion of the mounting surface of the TO-218 package be in contact with heat sink. This achieves maximum oversurface distance to prevent a high-voltage path over the device body to grounded heat sink.

General Mounting Notes

Care must be taken on both packages at all times to avoid strain to the tab or leads. For easy insertion of the part onto the board or heat sink, avoid axial strain on the leads. Carefully measure mounting holes for the tab and the leads, and do any forming of the tab or leads before mounting. Refer to the “Lead Form Dimensions” section of this catalog before attempting lead form operations.

Rivets may be used for less demanding and more economical applications. 1/8" all-aluminum pop rivets can be used on both TO-220 and TO-202 packages. Use a 0.129”-0.133” (#30) drill for the hole and insert the rivet from the top side, as shown in Figure AN1004.9. An insertion tool, similar to a “USM” PRG 430 hand riveter, is recommended. A wide selection of grip ranges is available, depending upon the thickness of the heat sink material. Use an appropriate grip range to securely anchor the device, yet not deform the mounting tab. The recommended rivet tool has a protruding nipple that will allow easy insertion of the rivet and keep the tool clear of the plastic case of the device.

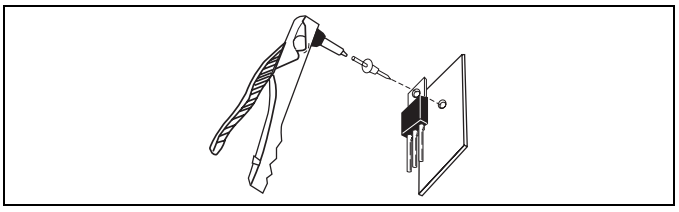


Figure AN1004.9 Pop Riveting Technique

A Milford #511 (Milford Group, Milford, CT) semi-tubular steel rivet set into a 0.129" receiving hole with a riveting machine similar to a Milford S256 is also acceptable. Contact the rivet machine manufacturer for exact details on application and set-up for optimum results.

Pneumatic or other impact riveting devices are not recommended due to the shock they may apply to the device.

Under no circumstance should any tool or hardware come into contact with the case. The case should not be used as a brace for any rotation or shearing force during mounting or in use. Non-standard size screws, nuts, and rivets are easily obtainable to avoid clearance problems.

Always use an accurate torque wrench to mount devices. No gain is achieved by overtorquing devices. In fact, overtorquing may cause the tab and case to deform or rupture, seriously damaging the device. The curve shown in Figure AN1004.10 illustrates the effect of proper torque.

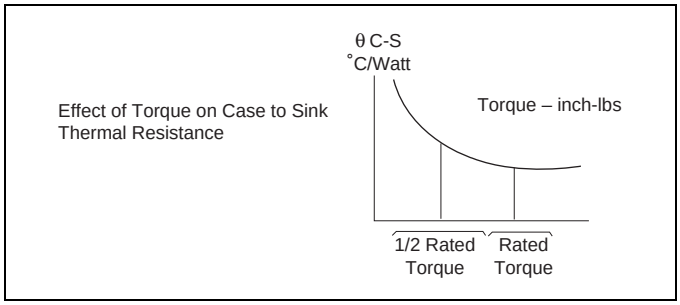


Figure AN1004.10 Effect of Torque to Sink Thermal Resistance

With proper care, the mounting tab of a device can be soldered to a surface. However, the heat required to accomplish this operation can damage or destroy the semiconductor chip or internal assembly. See “Surface Mount Soldering Recommendations” (AN1005) in this catalog.

Spring-steel clips can be used to replace torqued hardware in assembling thyristors to heat sinks. Clips snap into heat sink slots to hold the device in place for PC board insertion. Clips are available in several sizes for various heat sink thicknesses and thyristor case styles from *Aavid Thermalloy* in Concord, New Hampshire. A typical heatsink is shown in Figure AN1004.11

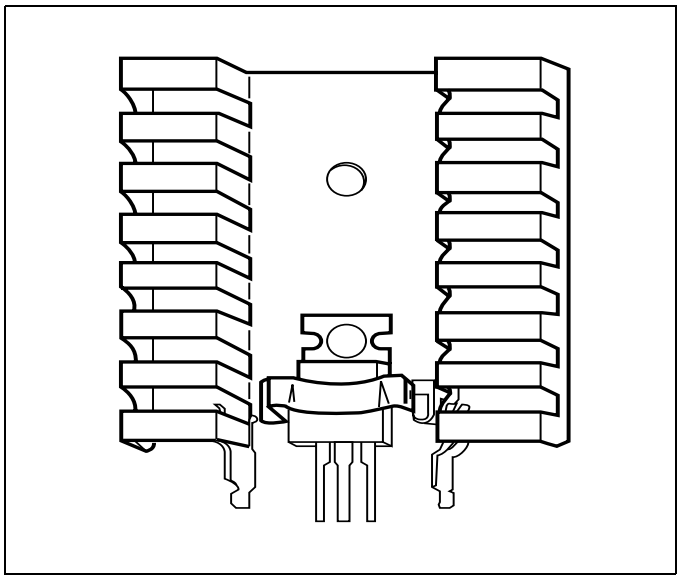


Figure AN1004.11 Typical Heat Sink Using Clips

Soldering Of Leads

A prime consideration in soldering leads is the soldering of device leads into PC boards, heat sinks, and so on. Significant damage can be done to the device through improper soldering. In any soldering process, do not exceed the data sheet lead solder temperature of +230 °C for 10 seconds, maximum, ≥1/16" from the case.

This application note presents details about the following three types of soldering:

- Hand soldering
- Wave soldering
- Dip soldering

Hand Soldering

This method is mostly used in prototype breadboarding applications and production of small modules. It has the greatest potential for misuse. The following recommendations apply to Teccor TO-92, TO-202, TO-220, and TO-218 packages.

Select a small- to medium-duty electric soldering iron of 25 W to 45 W designed for electrical assembly application. Tip temperature should be rated from 600 °F to 800 °F (300 °C to 425 °C). The iron should have sufficient heat capacity to heat the joint quickly and efficiently in order to minimize contact time to the part. Pencil tip probes work very well. Neither heavy-duty electrical irons of greater than 45 W nor flame-heated irons and large heavy tips are recommended, as the tip temperatures are far too high and uncontrollable and can easily exceed the time-temperature limit of the part.

Teccor Fastpak devices require a different soldering technique. Circuit connection can be done by either quick-connect terminals or solder.

Since most quick-connect 0.250” female terminals have a maximum rating of 30 A, connection to terminals should be made by soldering wires instead of quick-connects.

Recommended wire is 10 AWG stranded wire for use with MT1 and MT2 for load currents above 30 A. Soldering should be performed with a 100-watt soldering iron. The iron should not remain in contact with the wire and terminal longer than 40 seconds so the Fastpak triac is not damaged.

For the Teccor TO-218X package, the basic rules for hand soldering apply; however, a larger iron may be required to apply sufficient heat to the larger leads to efficiently solder the joint.

Remember not to exceed the lead solder temperatures of +230 °C for 10 seconds, maximum, ≥1/16" (1.59mm) from the case.

A 60/40 or 63/37 Sn/Pb solder is acceptable. This low melting-point solder, used in conjunction with a mildly activated rosin flux, is recommended.

Insert the device into the PC board and, if required, attach the device to the heat sink before soldering. Each lead should be individually heat sinked as it is soldered. Commercially available heat sink clips are excellent for this use. Hemostats may also be used if available. Needle-nose pliers are a good heat sink choice; however, they are not as handy as stand-alone type clips.

In any case, the lead should be clipped or grasped between the solder joint and the case, as near to the joint as possible. Avoid straining or twisting the lead in any way.

Use a clean pre-tinned iron, and solder the joint as quickly as possible. Avoid overheating the joint or bringing the iron or solder into contact with other leads that are not heat sinked.

Wave Solder

Wave soldering is one of the most efficient methods of soldering large numbers of PC boards quickly and effectively. Guidelines for soldering by this method are supplied by equipment manufacturers. The boards should be pre-heated to avoid thermal shock to semiconductor components, and the time-temperature cycle in the solder wave should be regulated to avoid heating the device beyond the recommended temperature rating. A mildly activated resin flux is recommended. Figure AN1004.12 shows typical heat and time conditions.

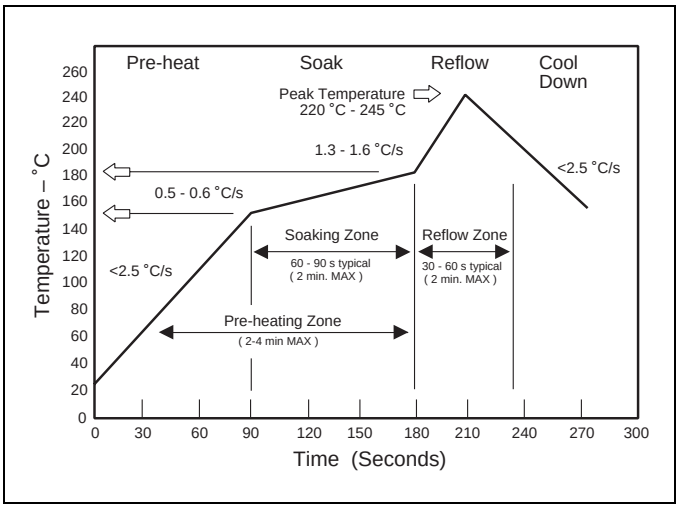


Figure AN1004.12 Reflow Soldering with Pre-heating

Dip Soldering

Dip soldering is very similar to wave soldering, but it is a hand operation. Follow the same considerations as for wave soldering, particularly the time-temperature cycle which may become operator dependent because of the wide process variations that may occur. This method is not recommended.

Board or device clean-up is left to the discretion of the customer. Teccor devices are tolerant of a wide variety of solvents, and they conform to MIL-STD 202E method 215 “Resistance to Solvents.”

Notes

AN1005

Surface Mount Soldering Recommendations

Introduction

The most important consideration in reliability is achieving a good solder bond between surface mount device (SMD) and substrate since the solder provides the thermal path from the chip. A good bond is less subject to thermal fatiguing and will result in improved device reliability.

The most economic method of soldering is a process in which all different components are soldered simultaneously, such as DO-214, Compak, TO-252 devices, capacitors, and resistors.

Reflow Of Soldering

The preferred technique for mounting microminiature components on hybrid thick- and thin-film is reflow soldering.

The DO-214 is designed to be mounted directly to or on thick-film metallization which has been screened and fired on a substrate. The recommended substrates are Alumina or P.C. Board material.

Recommended metallization is silver palladium or molymanganese (plated with nickel or other elements to enhance solderability). For more information, consult Du Pont's Thick-Film handbook or the factory.

It is best to prepare the substrate by either dipping it in a solder bath or by screen printing a solder paste.

After the substrate is prepared, devices are put in place with vacuum pencils. The device may be laid in place without special alignment procedures since it is self-aligning during the solder reflow process and will be held in place by surface tension.

For reliable connections, keep the following in mind:

(1) Maximum temperature of the leads or tab during the soldering cycle does not exceed 275 °C.
(2) Flux must affect neither components nor connectors.
(3) Residue of the flux must be easy to remove.

Good flux or solder paste with these properties is available on the market. A recommended flux is Alpha 5003 diluted with benzyl alcohol. Dilution used will vary with application and must be determined empirically.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place.

Because solder paste contains a flux, it has good inherent adhesive properties which eases positioning of the components. Allow flux to dry at room temperature or in a 70 °C oven. Flux should be dry to the touch. Time required will depend on flux used.

With the components in position, the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate, on a conveyor belt running through an infrared tunnel, or by using vapor phase soldering.

In the vapor phase soldering process, the entire PC board is uniformly heated within a vapor phase zone at a temperature of approximately 215 °C. The saturated vapor phase zone is obtained by heating an inert (inactive) fluid to the boiling point. The vapor phase is locked in place by a secondary vapor. (Figure AN1005.1) Vapor phase soldering provides uniform heating and prevents overheating.

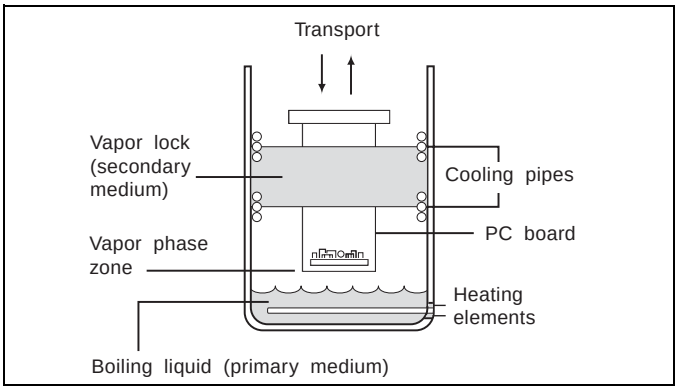


Figure AN1005.1 Principle of Vapor Phase Soldering

No matter which method of heating is used, the maximum allowed temperature of the plastic body must not exceed 250 °C during the soldering process. For additional information on temperature behavior during the soldering process, see Figure AN1005.2 and Figure AN1005.3.

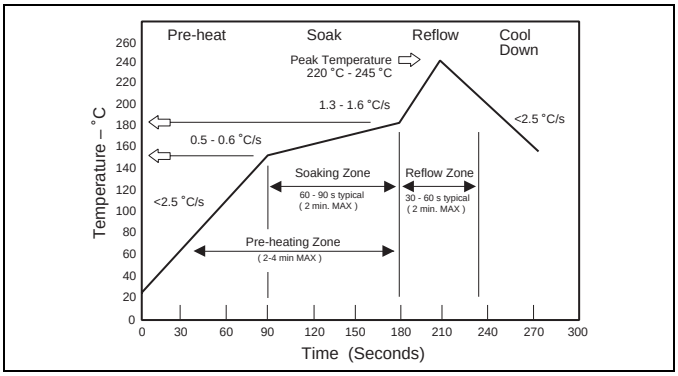


Figure AN1005.2 Reflow Soldering Profile

Reflow Soldering Zones

Zone 1: Initial Pre-heating Stage (25 °C to 150 °C)

- Excess solvent is driven off.
- PCB and Components are gradually heated up.
- Temperature gradient shall be <2.5 °C/Sec.

Zone 2: Soak Stage (150 °C to 180 °C)

- Flux components start activation and begin to reduce the oxides on component leads and PCB pads.
- PCB components are brought nearer to the temperature at which solder bonding can occur.
- Soak allows different mass components to reach the same temperature.
- Activated flux keeps metal surfaces from re-oxidizing.

Zone 3: Reflow Stage (180 °C to 235 °C)

- Paste is brought to the alloy's melting point.
- Activated flux reduces surface tension at the metal interface so metallurgical bonding occurs.

Zone 4: Cool-down Stage (180 °C to 25 °C)

Assembly is cooled evenly so thermal shock to the components or PCB is reduced.

The surface tension of the liquid solder tends to draw the leads of the device towards the center of the soldering area and so has a correcting effect on slight mispositionings. However, if the layout is not optimized, the same effect can result in undesirable shifts, particularly if the soldering areas on the substrate and the components are not concentrically arranged. This problem can be solved by using a standard contact pattern which leaves sufficient scope for the self-positioning effect (Figure AN1005.3 and Figure AN1005.4) Figure AN1005.5 shows the reflow soldering procedure.

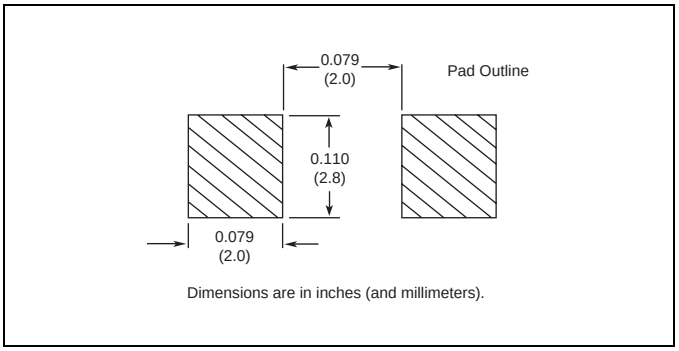


Figure AN1005.3 Minimum Required Dimensions of Metal Connection of Typical DO-214 Pads on Hybrid Thick- and Thin-film Substrates

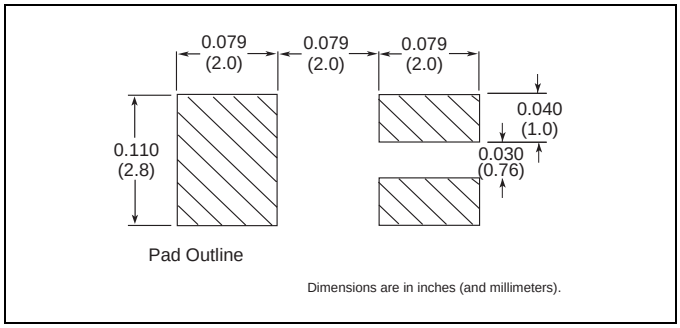


Figure AN1005.4 Modified DO-214 Compak — Three-leaded Surface Mount Package

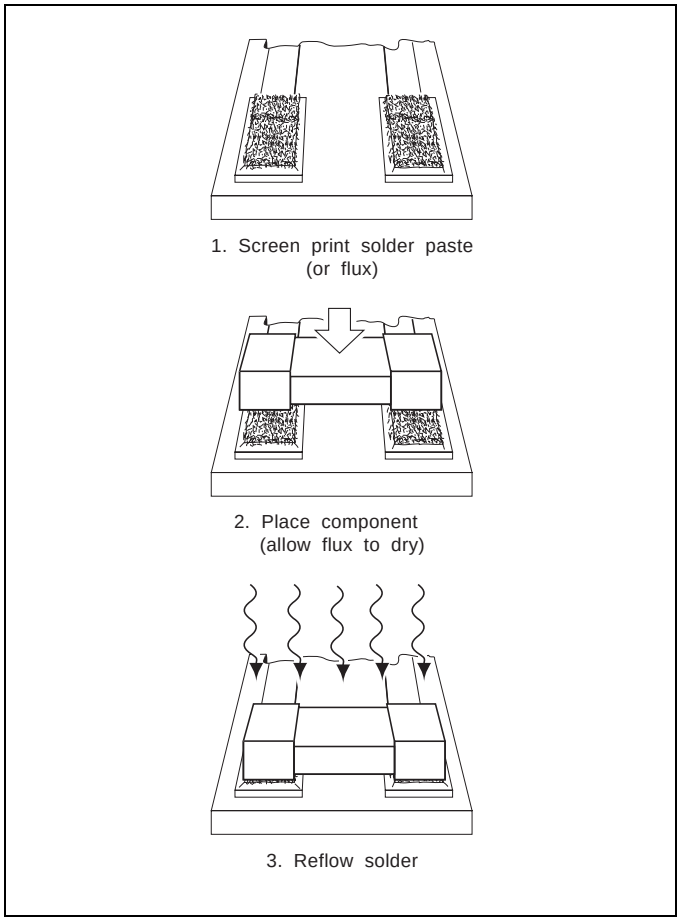


Figure AN1005.5 Reflow Soldering Procedure

After the solder is set and cooled, visually inspect the connections and, where necessary, correct with a soldering iron. Finally, the remnants of the flux must be removed carefully.

Use vapor degrease with an azeotrope solvent or equivalent to remove flux. Allow to dry.

After the drying procedure is complete, the assembly is ready for testing and/or further processing.

Wave Soldering

Wave soldering is the most commonly used method for soldering components in PCB assemblies. As with other soldering processes, a flux is applied before soldering. After the flux is applied, the surface mount devices are glued into place on a PC board. The board is then placed in contact with a molten wave of solder at a temperature between 240 °C and 260 °C, which affixes the component to the board.

Dual wave solder baths are also in use. This procedure is the same as mentioned above except a second wave of solder removes excess solder.

Although wave soldering is the most popular method of PCB assembly, drawbacks exist. The negative features include solder bridging and shadows (pads and leads not completely wetted) as board density increases. Also, this method has the sharpest thermal gradient. To prevent thermal shock, some sort of pre-heating device must be used. Figure AN1005.6 shows the procedure for wave soldering PCBs with surface mount devices only. Figure AN1005.7 shows the procedure for wave soldering PCBs with both surface mount and leaded components.

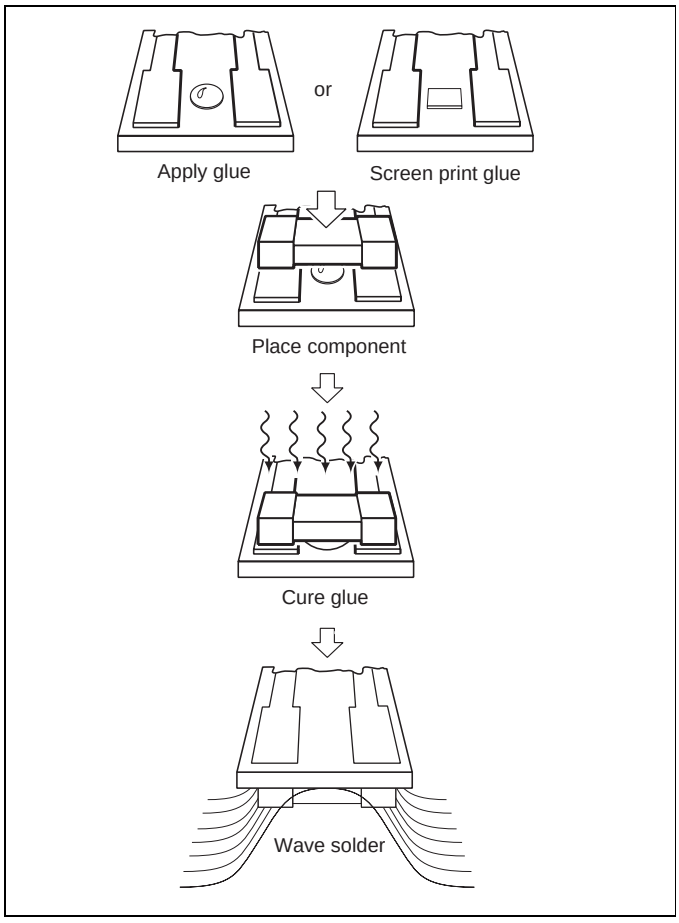


Figure AN1005.6 Wave Soldering PCBs With Surface Mount Devices Only

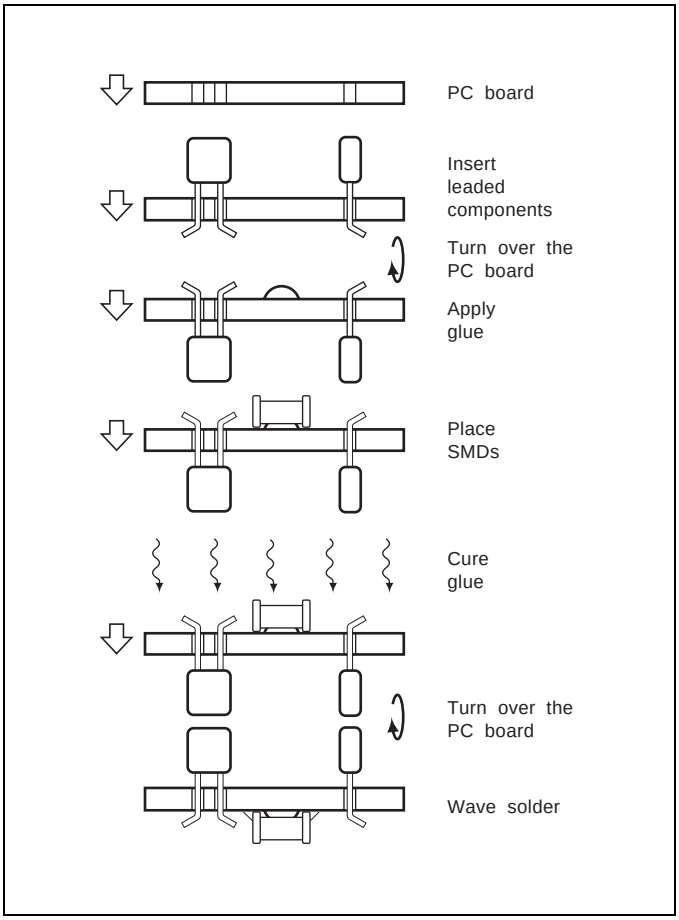


Figure AN1005.7 Wave Soldering PCBs With Both Surface Mount and Leaded Components

Immersion Soldering

Maximum allowed temperature of the soldering bath is 235 °C. Maximum duration of soldering cycle is five seconds, and forced cooling must be applied.

Hand Soldering

It is possible to solder the DO-214, Compak, and TO-252 devices with a miniature hand-held soldering iron, but this method has particular drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits.

Recommended Metal-alloy

(1) 63/37 Sn/Pb
(2) 60/40 Sn/Pb

Pre-Heating

Pre-heating is recommended for good soldering and to avoid damage to the DO-214, Compak, TO-252 devices, other components, and the substrate. Maximum pre-heating temperature is 165 °C while the maximum pre-heating duration may be 10 seconds. However, atmospheric pre-heating is permissible for several minutes provided temperature does not exceed 125 °C.

Gluing Recommendations

Prior to wave soldering, surface mount devices (SMDs) must be fixed to the PCB or substrate by means of an appropriate adhesive. The adhesive (in most cases a multicomponent adhesive) has to fulfill the following demands:

- Uniform viscosity to ensure easy coating
- No chemical reactions upon hardening in order not to deteriorate component and PC board
- Straightforward exchange of components in case of repair

Low-temperature Solder for Reducing PC Board Damage

In testing and troubleshooting surface-mounted components, changing parts can be time consuming. Moreover, desoldering and soldering cycles can loosen and damage circuit-board pads. Use low-temperature solder to minimize damage to the PC board and to quickly remove a component. One low-temperature alloy is indium-tin, in a 50/50 mixture. It melts between 118 °C and 125 °C, and tin-lead melts at 183 °C. If a component needs replacement, holding the board upside down and heating the area with a heat gun will cause the component to fall off. Performing the operation quickly minimizes damage to the board and component.

Proper surface preparation is necessary for the In-Sn alloy to wet the surface of the copper. The copper must be clean, and you must add flux to allow the alloy to flow freely.You can use rosin dissolved in alcohol. Perform the following steps:

(1) Cut a small piece of solder and flow it onto one of the pads.

(2) Place the surface-mount component on the pad and melt the soldered pad to its pin while aligning the part. (This operation places all the pins flat onto their pads.)

(3) Cut small pieces of the alloy solder and flow each piece onto each of the other legs of the component.

Indium-tin solder is available from ACI Alloys, San Jose, CA and Indium Corporation of America, Utica, NY.

Multi-use Footprint

Package soldering footprints can be designed to accommodate more than one package. Figure AN1005.8 shows a footprint design for using both the Compak and an SOT-223. Using the dual pad outline makes it possible to use more than one supplier source.

Cleaning Recommendations

Using solvents for PC board or substrate cleaning is permitted from approximately 70 °C to 80 °C.

The soldered parts should be cleaned with azeotrope solvent followed by a solvent such as methol, ethyl, or isopropyl alcohol.

Ultrasonic cleaning of surface mount components on PCBs or substrates is possible.

The following guidelines are recommended when using ultrasonic cleaning:

- Cleaning agent: Isopropanol
- Bath temperature: approximately 30 °C
- Duration of cleaning: MAX 30 seconds
- Ultrasonic frequency: 40 kHz
- Ultrasonic changing pressure: approximately 0.5 bar

Cleaning of the parts is best accomplished using an ultrasonic cleaner which has approximately 20 W of output per one liter of solvent. Replace the solvent on a regular basis.

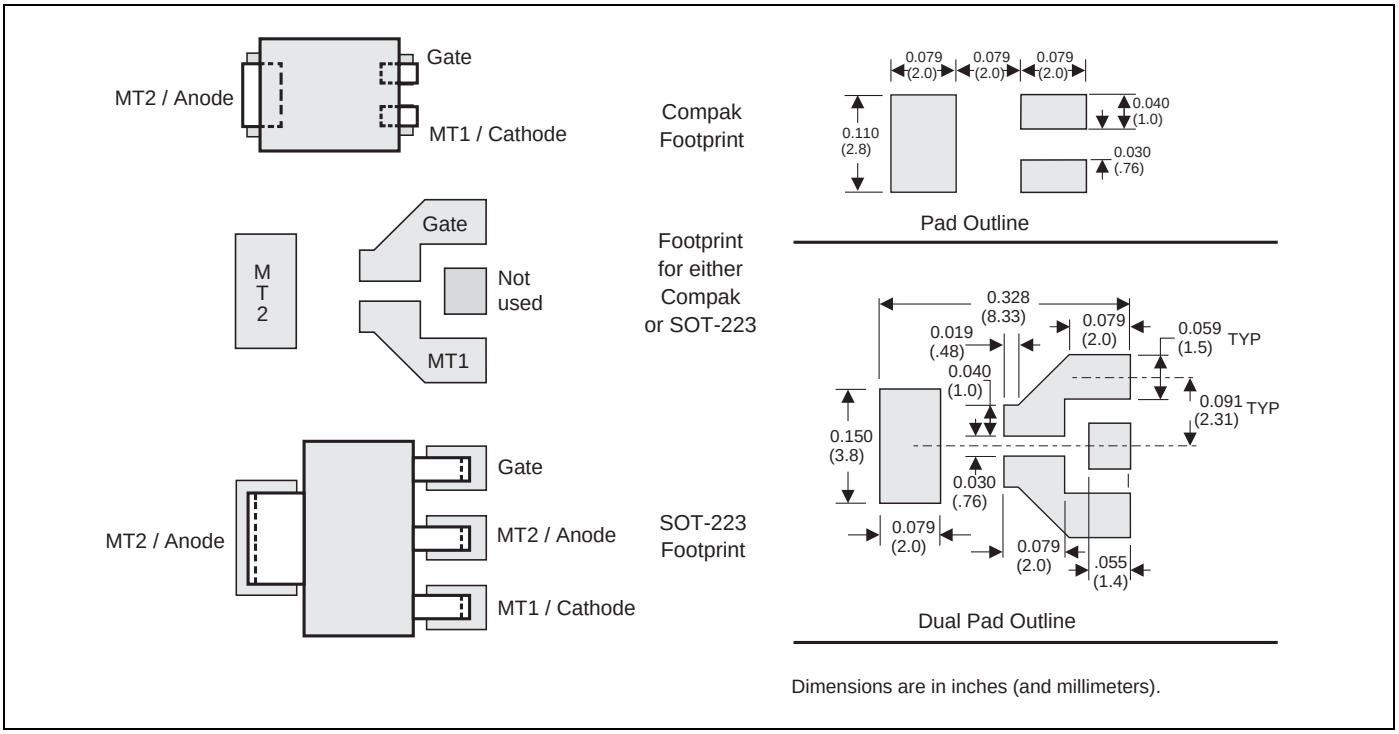


Figure AN1005.8 Dual Footprint for *Compak* Package

AN1006

Testing Teccor Semiconductor Devices Using Curve Tracers

Introduction

One of the most useful and versatile instruments for testing semiconductor devices is the curve tracer (CT). Tektronix is the best known manufacturer of curve tracers and produces four basic models: 575, 576, 577 and 370. These instruments are specially adapted CRT display screens with associated electronics such as power supplies, amplifiers, and variable input and output functions that allow the user to display the operating characteristics of a device in an easy-to-read, standard graph form. Operation of Tektronix CTs is simple and straightforward and easily taught to non-technical personnel. Although widely used by semiconductor manufacturers for design and analytical work, the device consumer will find many uses for the curve tracer, such as incoming quality control, failure analysis, and supplier comparison. Curve tracers may be easily adapted for go-no go production testing. Tektronix also supplies optional accessories for specific applications along with other useful hardware.

Tektronix Equipment

Although Tektronix no longer produces curve tracer model 575, many of the units are still operating in the field, and it is still an extremely useful instrument. The 576, 577 and 370 are current curve tracer models and are more streamlined in their appearance and operation. The 577 is a less elaborate version of the 576, yet retains all necessary test functions.

The following basic functions are common to all curve tracers:

- **Power supply** supplies positive DC voltage, negative DC voltage, or AC voltage to bias the device. Available power is varied by limiting resistors.
- **Step generator** supplies current or voltage in precise steps to control the electrode of the device. The number, polarity, and frequency of steps are selectable.
- **Horizontal amplifier** displays power supply voltage as applied to the device. Scale calibration is selectable.
- **Vertical amplifier** displays current drawn from the supply by the device. Scale calibration is selectable.

Curve tracer controls for beam position, calibration, pulse operation, and other functions vary from model to model. The basic theory of operation is that for each curve one terminal is driven with a constant voltage or current and the other one is swept with a half sinewave of voltage. The driving voltage is stepped through several values, and a different trace is drawn on each sweep to generate a family of curves.

Limitations, Accuracy, and Correlation

Although the curve tracer is a highly versatile device, it is not capable of every test that one may wish to perform on semiconductor devices such as dv/dt, secondary reverse breakdown, switching speeds, and others. Also, tests at very high currents and/or voltages are difficult to conduct accurately and without damaging the devices. A special high-current test fixture available from Tektronix can extend operation to 200 A pulsed peak. Kelvin contacts available on the 576 and 577 eliminate inaccuracy in voltage measured at high current (V_{TM}) by sensing voltage drop due to contact resistance and subtracting from the reading.

Accuracy of the unit is within the published manufacturer's specification. Allow the curve tracer to warm up and stabilize before testing begins. Always expand the horizontal or vertical scale as far as possible to increase the resolution. Be judicious in recording data from the screen, as the trace line width and scale resolution factor somewhat limit the accuracy of what may be read. Regular calibration checks of the instrument are recommended. Some users keep a selection of calibrated devices on hand to verify instrument operation when in doubt. Re-calibration or adjustment should be performed only by qualified personnel.

Often discrepancies exist between measurements taken on different types of instrument. In particular, most semiconductor manufacturers use high-speed, computerized test equipment to test devices. They test using very short pulses. If a borderline unit is then measured on a curve tracer, it may appear to be out of specification. The most common culprit here is heat. When a semiconductor device increases in temperature due to current flow, certain characteristics may change, notably gate characteristics on SCRs, gain on transistors, leakage, and so on. It is very difficult to operate the curve tracer in such a way as to eliminate the heating effect. Pulsed or single-trace operation helps reduce this problem, but care should be taken in comparing curve tracer measurements to computer tests. Other factors such as stray capacitances, impedance matching, noise, and device oscillation also may create differences.

Safety (Cautions and Warnings)

Adhere rigidly to Tektronix safety rules supplied with each curve tracer. No attempt should be made to defeat any of the safety interlocks on the device as the curve tracer can produce a lethal shock. Also, older 575 models do not have the safety interlocks as do the new models. Take care never to touch any device or open the terminal while energized.

WARNING: Devices on the curve tracer may be easily damaged from electrical overstress.

Follow these rules to avoid destroying devices:

- Familiarize yourself with the expected maximum limits of the device.
- Limit the current with the variable resistor to the minimum necessary to conduct the test.
- Increase power slowly to the specified limit.
- Watch for device “runaway” due to heating.
- Apply and increase gate or base drive slowly and in small steps.
- Conduct tests in the minimum time required.

General Test Procedures

Read all manuals before operating a curve tracer.

Perform the following manufacturer’s equipment check:

1. Turn on and warm up curve tracer, but turn off, or down, all power supplies.
2. Correctly identify terminals of the device to be tested. Refer to the manufacturer’s guide if necessary.
3. Insert the device into the test fixture, matching the device and test terminals.
4. Remove hands from the device and/or close interlock cover.
5. Apply required bias and/or drive.
6. Record results as required.
7. Disconnect all power to the device before removing.

Model 576 Curve Tracer Procedures

The following test procedures are written for use with the model 576 curve tracer. (Figure AN1006.1)

See “Model 370 Curve Tracer Procedure Notes” on page AN1006-16 and “Model 577 Curve Tracer Procedure Notes” on page AN1006-18 for setting adjustments required when using model 370 and 577 curve tracers.

The standard 575 model lacks AC mode, voltage greater than 200 V, pulse operations, DC mode, and step offset controls. The 575 MOD122C does allow voltage up to 400 V, including 1500 V in an AC mode. Remember that at the time of design, the 575 was built to test only transistors and diodes. Some ingenuity, experience, and external hardware may be required to test other types of devices.

For further information or assistance in device testing on Tektronix curve tracers, contact the Teccor Applications Engineering group.

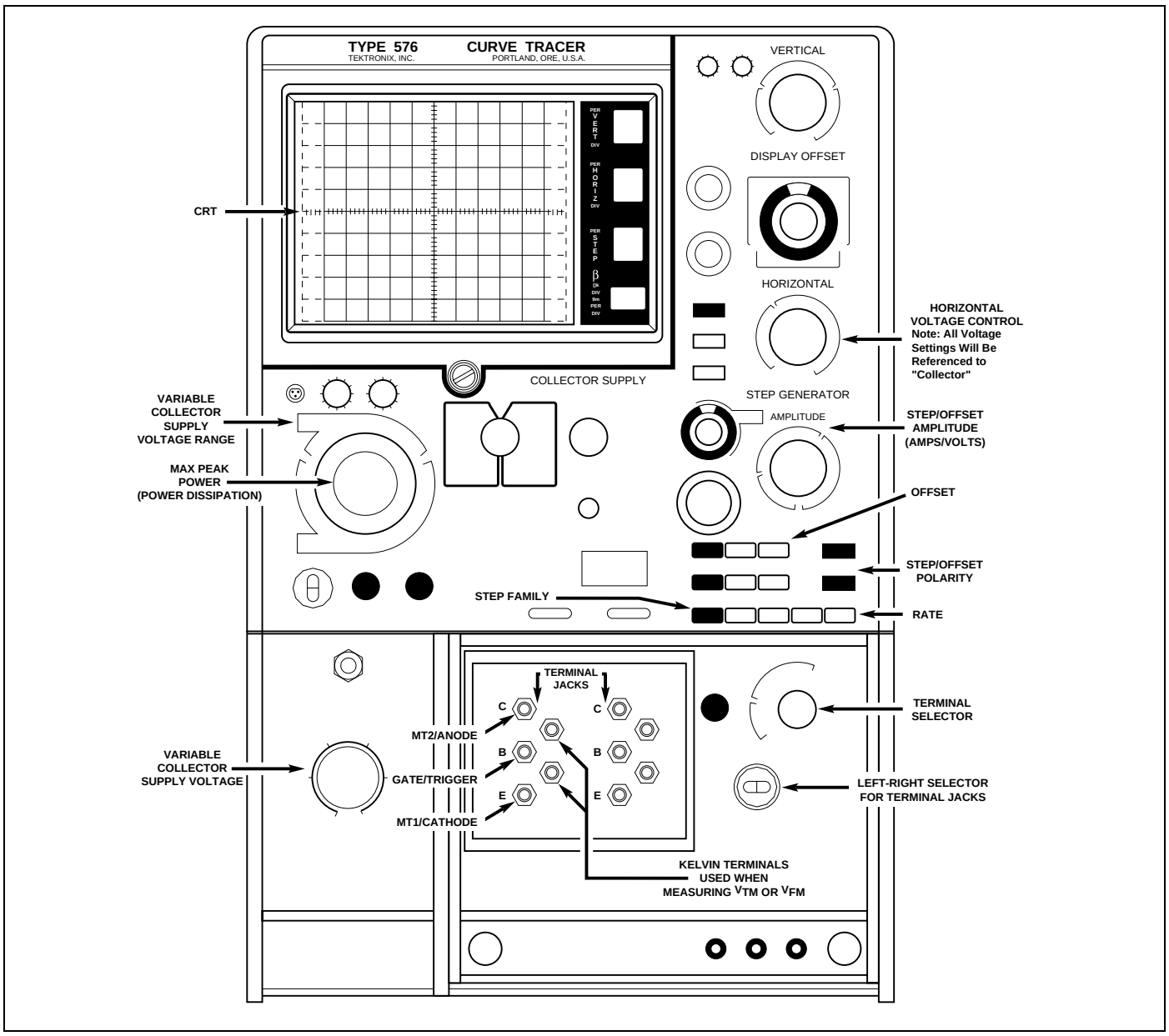


Figure AN1006.1 Tektronix Model 576 Curve Tracer

Power Rectifiers

The rectifier is a unidirectional device which conducts when forward voltage (above 0.7 V) is applied.

To connect the rectifier:

1. Connect *Anode* to *Collector Terminal (C)*.
2. Connect *Cathode* to *Emitter Terminal (E)*.

To begin testing, perform the following procedures.

Procedure 1: V_{RRM} and I_{RM}

To measure the V_{RRM} and I_{RM} parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 V.* (*2000 V* on 370)
2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level (*100 V/DIV* for 400 V and 600 V devices and *50 V/DIV* for 200 V devices).
3. Set **Mode** to *Leakage.*
4. Set **Vertical** knob to *100 µA/DIV.* (Due to leakage setting, the CRT readout will be 100 nA per division.)
5. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
6. Set **Polarity** to (–).
7. Set **Power Dissipation** to *2.2 W.* (*2 W* on 370)
8. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
9. Increase **Variable Collector Supply Voltage** to the rated V_{RRM} of the device and observe the dot on the CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.2)

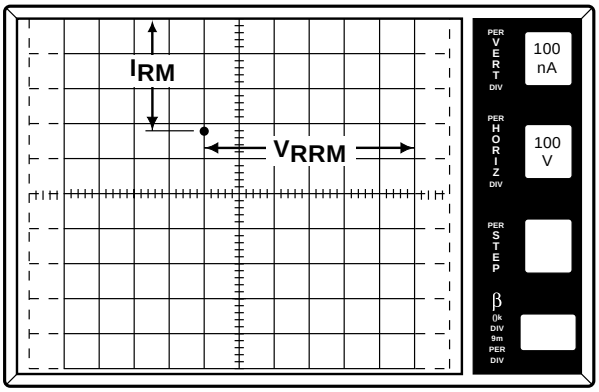


Figure AN1006.2 I_{RM} = 340 nA at V_{RRM} = 600 V

Procedure 2: V_{FM}

Before testing, note the following:

- A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of VFM will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connections.
- Due to the current limitations of standard curve tracer model 576, V_{FM} cannot be tested at rated current without a Tektronix model 176 high-current module. The procedure below is done at $I_{T(RMS)}$ = 10 A (20 A_{PK}). This test parameter allows the use of a standard curve tracer and still provides an estimate of whether V_{FM} is within specification.

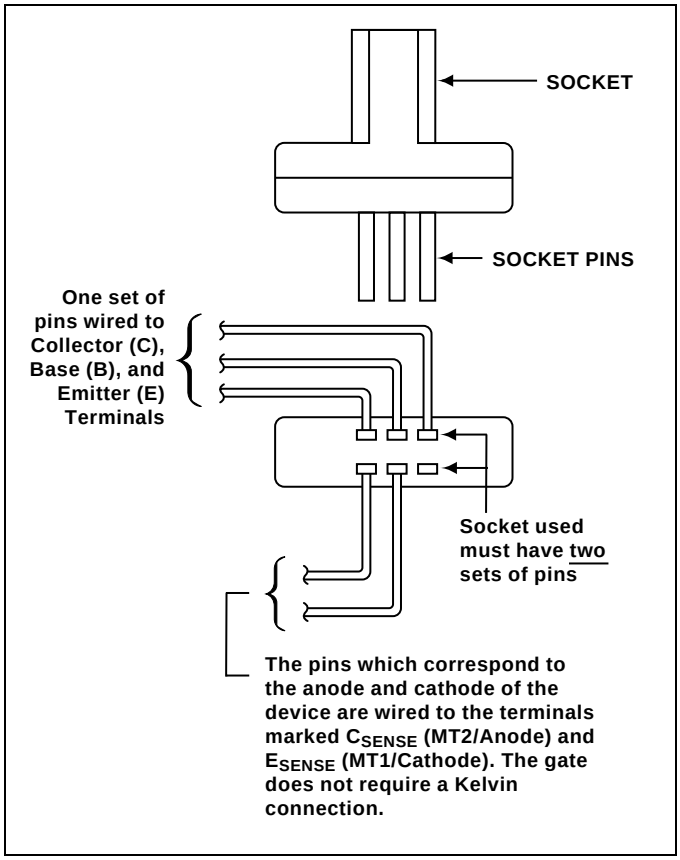


Figure AN1006.3 Instructions for Wiring Kelvin Socket

To measure the V_{FM} parameter:

1. Set **Variable Collector Supply Voltage Range** to *15 Max Peak Volts*. (*16 V* on 370)
2. Set **Horizontal** knob to *0.5 V/DIV.*
3. Set **Mode** to *Norm.*
4. Set **Vertical** knob to *2 A/DIV.*
5. Set **Power Dissipation** to *220 W* (*100 W* on 577).
6. Set **Polarity** to (+).
7. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
8. Increase **Variable Collector Supply Voltage** until current reaches 20 A.

WARNING: Limit test time to 15 seconds maximum.

To measure V_{FM}, follow along horizontal scale to the point where the trace crosses the 20 A axis. The distance from the left-hand side of scale to the crossing point is the V_{FM} value. (Figure AN1006.4)

Note: Model 370 current is limited to 10 A.

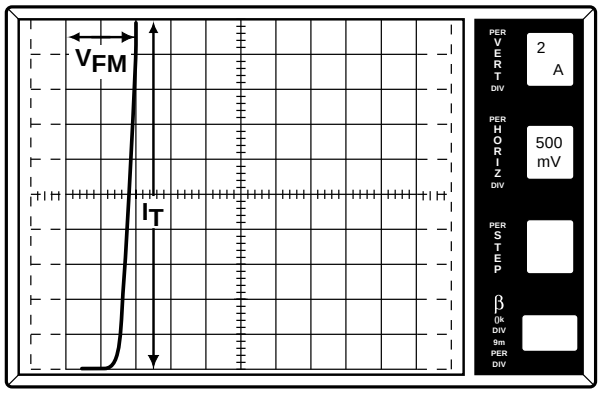


Figure AN1006.4 V_{FM} = 1 V at I_{PK} = 20 A

SCRs

SCRs are half-wave unidirectional rectifiers turned on when current is supplied to the gate terminal. If the current supplied to the gate is to be in the range of 12 µA and 500 µA, then a sensitive SCR is required; if the gate current is between 1 mA and 50 mA, then a non-sensitive SCR is required.

To connect the rectifier:

1. Connect *Anode* to *Collector Terminal (C)*.
2. Connect *Cathode* to *Emitter Terminal (E)*.

Note: When sensitive SCRs are being tested, a 1 kΩ resistor must be connected between the gate and the cathode, except when testing I_{GT}.

To begin testing, perform the following procedures.

Procedure 1: V_{DRM}, V_{RRM}, I_{DRM}, I_{RRM}

To measure the V_{DRM}, V_{RRM}, I_{DRM}, and I_{RRM} parameter:

1. Set **Variable Collector Supply Voltage Range** to appropriate *Max Peak Volts* for device under test. (Value selected should be equal to or greater than the device's V_{DRM} rating.)
2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level. (The *100 V/DIV* scale should be used for testing devices having a V_{DRM} value of 600 V or greater; the *50 V/DIV* scale for testing parts rated from 300 V to 500 V, and so on.)
3. Set **Mode** to *Leakage*.
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
7. Set **Vertical** knob to approximately ten times the maximum leakage current (I_{DRM}, I_{RRM}) specified for the device. (For sensitive SCRs, set to *50 µA*.)

Note: The CRT screen readout should show 1% of the maximum leakage current if the vertical scale is divided by 1,000 when leakage current mode is used.

Procedure 2: V_{DRM}, I_{DRM}

To measure the V_{DRM} and I_{DRM} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
2. Set **Variable Collector Supply Voltage** to the rated V_{DRM} of the device and observe the dot on CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.5)

WARNING: Do NOT exceed V_{DRM}/V_{RRM} rating of SCRs, triacs, or *Quadracs*. These devices can be damaged.

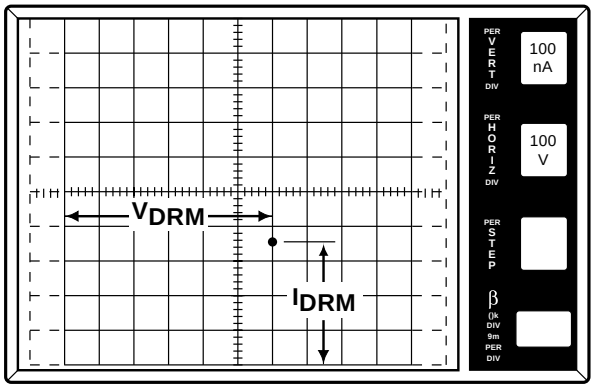


Figure AN1006.5 I_{DRM} = 350 nA at V_{DRM} = 600 V

Procedure 3: V_{RRM}, I_{RRM}

To measure the V_{RRM} and I_{RRM} parameter:

1. Set **Polarity** to (–).
2. Repeat Steps 1 and 2 (V_{DRM}, I_{DRM}) except substitute V_{RRM} value for V_{DRM}. (Figure AN1006.6)

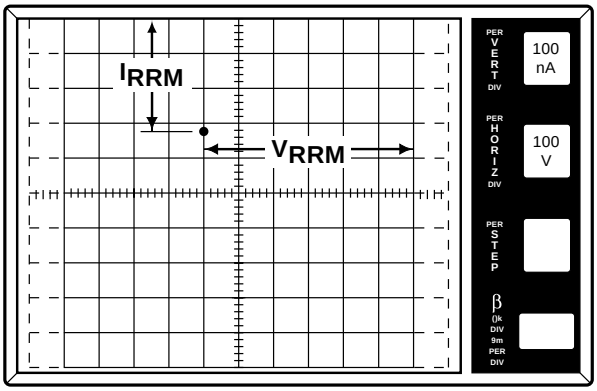


Figure AN1006.6 I_{RRM} = 340 nA at V_{RRM} = 600 V

Procedure 4: V_{TM}

To measure the V_{TM} parameter:

1. Set **Terminal Selector** to *Step Generator-Emitter Grounded*.
2. Set **Polarity** to *(+)*.
3. Set **Step/Offset Amplitude** to twice the maximum I_{GT} rating of the device (to ensure the device turns on). For sensitive SCRs, set to *2 mA*.
4. Set **Max Peak Volts** to *15 V.* (*16 V* on 370)
5. Set **Offset** by depressing *0* (zero).

6. Set **Rate** by depressing *Norm*.
7. Set **Step Family** by depressing *Rep* (repetitive).
8. Set **Mode** to *DC*.
9. Set **Horizontal** knob to *0.5 V/DIV*.
10. Set **Power Dissipation** to *220 W* (*100 W* on 577).
11. Set **Number of Steps** to *1*. (Set steps to *0* (zero) on 370.)
12. Set **Vertical** knob to a sufficient setting to allow the viewing of 2 times the $I_{T(RMS)}$ rating of the device ($I_{T(peak)}$) on CRT.

    Before continuing with testing, note the following:

    (1) Due to the excessive amount of power that can be generated in this test, only parts with an $I_{T(RMS)}$ rating of 6 A or less should be tested on standard curve tracer. If testing devices above 6 A, a Tektronix model 176 high-current module is required.

    (2) A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in the fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connectors.
13. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
14. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$, which is twice the $I_{T(RMS)}$ rating of the-SCR under test.

Note: Model 370 current is limited to 10 A.

WARNING: Limit test time to 15 seconds maximum after the *Variable Collector Supply* has been set to $I_{T(peak)}$, After the *Variable Collector Supply Voltage* has been set to $I_{T(peak)}$, the test time can automatically be shortened by changing *Step Family* from repetitive to single by depressing the *Single* button.

To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. The distance from the left-hand side of scale to the intersection point is the V_{TM} value. (Figure AN1006.7)

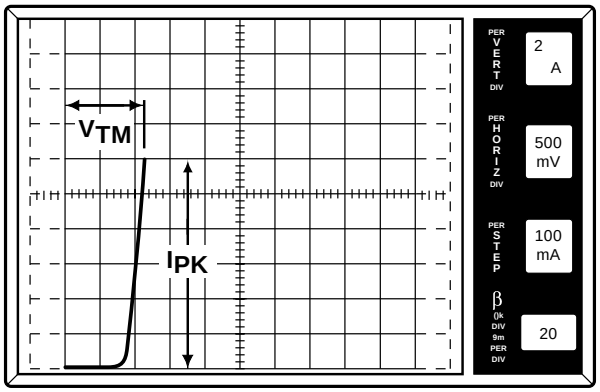


Figure AN1006.7 V_{TM} = 1.15 V at $I_{T(peak)}$ = 12 A

Procedure 5: I_H

To measure the I_H parameter:

1. Set **Polarity** to *(+)*.
2. Set **Power Dissipation** to *2.2 W.* (*2 W* on 370)
3. Set **Max Peak Volts** to *75 V.* (80 V on 370)
4. Set **Mode** to *DC*.
5. Set **Horizontal** knob to *Step Generator.*
6. Set **Vertical** knob to approximately 10 percent of the maximum I_H specified.

   Note: Due to large variation of holding current values, the scale may have to be adjusted to observe holding current.
7. Set **Number of Steps** to *1*.
8. Set **Offset** by depressing *0* (zero). (Press *Aid* and *Oppose* at the same time on 370.)
9. Set **Step/Offset Amplitude** to twice the maximum I_{GT} of the device.
10. Set **Terminal Selector** to *Step Generator-Emitter Grounded.*
11. Set **Step Family** by depressing *Single*.
12. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
13. Increase **Variable Collector Supply Voltage** to maximum position (*100*).
14. Set **Step Family** by depressing *Single.* (This could possibly cause the dot on CRT to disappear, depending on the vertical scale selected.)
15. Change **Terminal Selector** from *Step Generator-Emitter Grounded* to *Open Base-Emitter Grounded*.
16. Decrease **Variable Collector Supply Voltage** to the point where the line on the CRT changes to a dot. The position of the beginning point of the line, just before the line becomes a dot, represents the holding current value. (Figure AN1006.8)

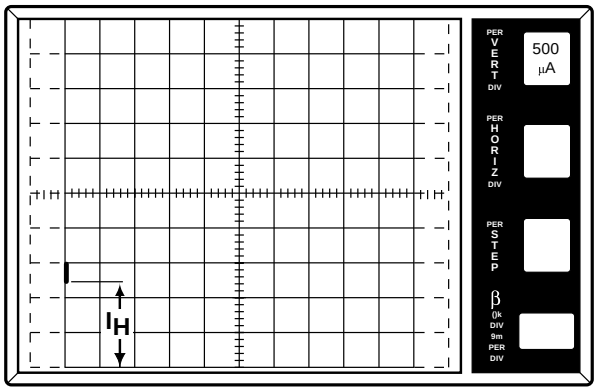


Figure AN1006.8 I_H = 1.2 mA

Procedure 6: I_{GT} and V_{GT}

To measure the I_{GT} and V_{GT} parameter:

1. Set **Polarity** to (+).
2. Set **Number of Steps** to *1*.
3. Set **Offset** by depressing *Aid*.
4. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and *Oppose* at the same time on 370.)
5. Set **Terminal Selector** to *Step Generator-Emitter Grounded.*
6. Set **Mode** to *Norm*.
7. Set **Max Peak Volts** to *15 V.* (*16 V* on 370)

8. Set **Power Dissipation** to *2.2 W.* (*2 W* on 370) For sensitive SCRs, set at 0.5 W. (*0.4 W* on 370)
9. Set **Horizontal** knob to *2 V/DIV.*
10. Set **Vertical** knob to *50 mA/DIV.*
11. Increase **Variable Collector Supply Voltage** until voltage reaches 12 V on CRT.
12. After 12 V setting is completed, change **Horizontal** knob to *Step Generator.*

Procedure 7: I_{GT}

To measure the I_{GT} parameter:

1. Set **Step/Offset Amplitude** to 20% of maximum rated I_{GT}.

   Note: R_{GK} should be removed when testing I_{GT}.
2. Set **Left-Right Terminal Jack Selector** to correspond with location of the test fixture.
3. Gradually increase **Offset Multiplier** until device reaches the conduction point. (Figure AN1006.9) Measure I_{GT} by following horizontal axis to the point where the vertical line crosses axis. This measured value is I_{GT}. (On 370, I_{GT} will be numerically displayed on screen under offset value.)

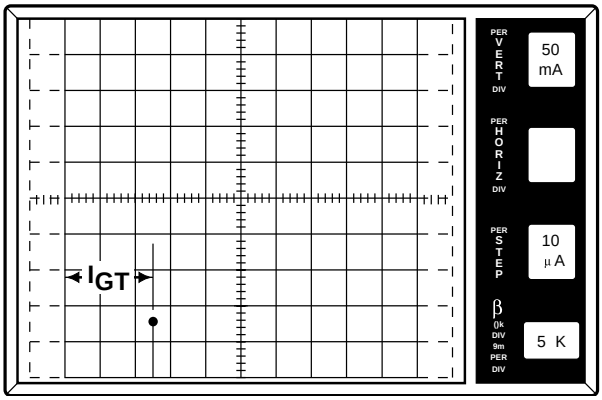


Figure AN1006.9 I_{GT} = 25 µA

Procedure 8: V_{GT}

To measure the V_{GT} parameter:

1. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and O*ppose* at the same time on 370.)
2. Set **Step Offset Amplitude** to 20% rated V_{GT}.
3. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
4. Gradually increase **Offset Multiplier** until device reaches the conduction point. (Figure AN1006.10) Measure V_{GT} by following horizontal axis to the point where the vertical line crosses axis. This measured value is V_{GT}. (On 370, V_{GT} will be numerically displayed on screen, under offset value.)

Procedure 9: $_{GT}$ will be numerically displayed on screen under offset value.)

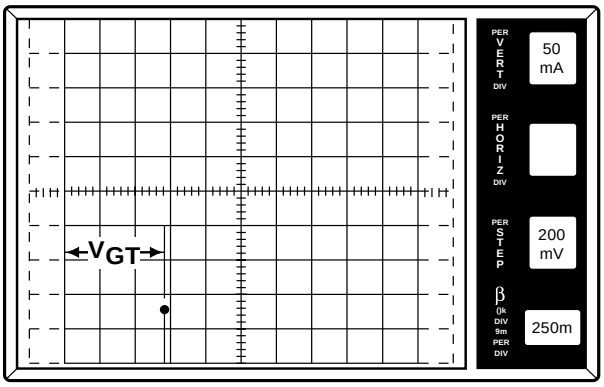


Figure AN1006.10 V_{GT} = 580 mV

Triacs

Triacs are full-wave bidirectional AC switches turned on when current is supplied to the gate terminal of the device. If gate control in all four quadrants is required, then a sensitive gate triac is needed, whereas a standard triac can be used if gate control is only required in Quadrants I through III.

To connect the triac:

1. Connect the *Gate* to the *Base Terminal* (B).
2. Connect *MT1* to the *Emitter Terminal* (E).
3. Connect *MT2* to the *Collector Terminal* (C).

To begin testing, perform the following procedures.

Procedure 1: $(+)V_{DRM}$, $(+)I_{DRM}$, $(-)V_{DRM}$, $(-)I_{DRM}$

Note: The (+) and (-) symbols are used to designate the polarity MT2 with reference to MT1.

To measure the $(+)V_{DRM}$, $(+)I_{DRM}$, $(-)V_{DRM}$, and $(-)I_{DRM}$ parameter:

1. Set **Variable Collector Supply Voltage Range** to appropriate *Max Peak Volts* for device under test. (Value selected should be equal to the device's V_{DRM} rating.)

   WARNING: Do NOT exceed V_{DRM}/V_{RRM} rating of SCRs, triacs, or *Quadracs*. These devices can be damaged.
2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level. (The *100 V/DIV* scale should be used for testing devices having a V_{DRM} rating of 600 V or greater; the *50 V/DIV* scale for testing parts rated from 30 V to 500 V, and so on.)
3. Set **Mode** to *Leakage*.
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
7. Set **Vertical** knob to ten times the maximum leakage current (I_{DRM}) specified for the device.

   Note: The CRT screen readout should show 1% of the maximum leakage current. The vertical scale is divided by 1,000 when leakage mode is used.

Procedure 2: (+)V_{DRM}, (+)I_{DRM}

To measure the (+)V_{DRM} and (+)I_{DRM} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with location of the test fixture.
2. Increase **Variable Collector Supply Voltage** to the rated V_{DRM} of the device and observe the dot on the CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.11)

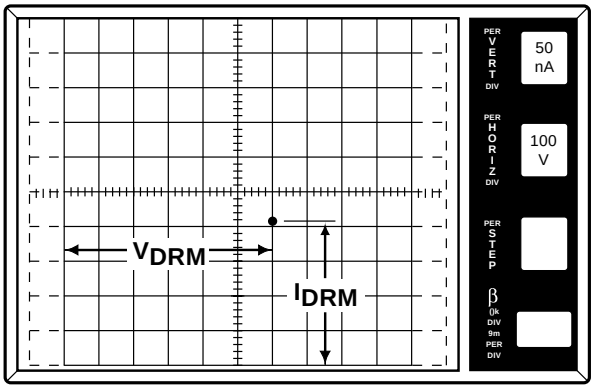


Figure AN1006.11 (+)I_{DRM} = 205 nA at (+)V_{DRM} = 600 V

Procedure 3: (-)V_{DRM}, (-)I_{DRM}

To measure the (-)V_{DRM} and (-)I_{DRM} parameter:

1. Set **Polarity** to (–).
2. Repeat Procedures 1 and 2. (Read measurements from upper right corner of the screen.)

Procedure 4: V_{TM} (Forward and Reverse)

To measure the $V_{TM\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Terminal Selector** to *Step Generator-Emitter Grounded*.
2. Set **Step/Offset Amplitude** to twice the maximum I_{GT} rating of the device (to insure the device turns on).
3. Set **Variable Collector Supply Voltage Range** to *15 V Max Peak volts*. (*16 V* on 370)
4. Set **Offset** by depressing *0* (zero).
5. Set **Rate** by depressing *Norm.*
6. Set **Step Family** by depressing *Rep* (Repetitive).
7. Set **Mode** to *Norm*.
8. Set **Horizontal** knob to *0.5 V/DIV.*
9. Set **Power Dissipation** to *220 W* (*100 W* on 577).
10. Set **Number of Steps** to *1*.
11. Set **Step/Offset Polarity** to non-inverted (button extended; on 577 button depressed).
12. Set **Vertical** knob to a sufficient setting to allow the viewing of 1.4 times the $I_{T(RMS)}$ rating of the device [$I_{T(peak)}$ on CRT].

Note the following:

- Due to the excessive amount of power that can be generated in this test, only parts with an $I_{T(RMS)}$ rating of 8 A or less should be tested on standard curve tracer. If testing devices above 8 A, a Tektronix model 176 high-current module is required.
- A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connections.

Procedure 5: $V_{TM\ (Forward)}$

To measure the $V_{TM\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$, which is 1.4 times $I_{T(RMS)}$ rating of the triac under test.

Note: Model 370 current is limited to 10 A.

WARNING: Limit test time to 15 seconds maximum. After the *Variable Collector Supply Voltage* has been set to $I_{T(peak)}$, the test time can automatically be set to a short test time by changing *Step Family* from repetitive to single by depressing the *Single* button.

To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. The distance from the left-hand side of scale to the crossing point is the V_{TM} value. (Figure AN1006.12)

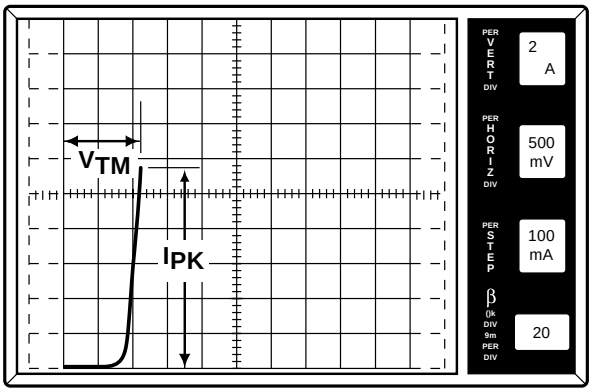


Figure AN1006.12 $V_{TM\ (forward)}$ = 1.1 V at I_{PK} = 11.3 A (8 A rms)

Procedure 6: $V_{TM\ (Reverse)}$

To measure the $V_{TM\ (Reverse)}$ parameter:

1. Set **Polarity** to (–).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$.
4. Measure $V_{TM(Reverse)}$ similar to Figure AN1006.12, except from upper right hand corner of screen.

Procedure 7: $I_{H(Forward\ and\ Reverse)}$

To measure the $I_{H\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Step/Offset Amplitude** to twice the I_{GT} rating of the device.
2. Set **Power Dissipation** to *10 W.*

3. Set **Max Peak Volts** to *75 V.* (*80 V* on 370)
4. Set **Mode** to *DC*.
5. Set **Horizontal** knob to *Step Generator*.
6. Set **Vertical** knob to approximately 10% of the maximum I_H specified.

   Note: Due to large variation of holding current values, the scale may have to be adjusted to observe holding current.
7. Set **Number of Steps** to *1*.
8. Set **Step/Offset Polarity** to non-inverted (button extended, on 577 button depressed).
9. Set **Offset** by depressing *0* (zero). (Press *Aid* and O*ppose* at same time on 370.)
10. Set **Terminal Selector** to *Step Generator-Emitter Grounded*.

Procedure 8: $I_{H(Forward)}$

To measure the $I_{H\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Increase **Variable Collector Supply Voltage** to maximum position (*100*).
4. Set **Step Family** by depressing *Single*.

   This could possibly cause the dot on the CRT to disappear, depending on the vertical scale selected).
5. Decrease **Variable Collector Supply Voltage** to the point where the line on the CRT changes to a dot. The position of the beginning point of the line, just before the line becomes a dot, represents the holding current value. (Figure AN1006.13)

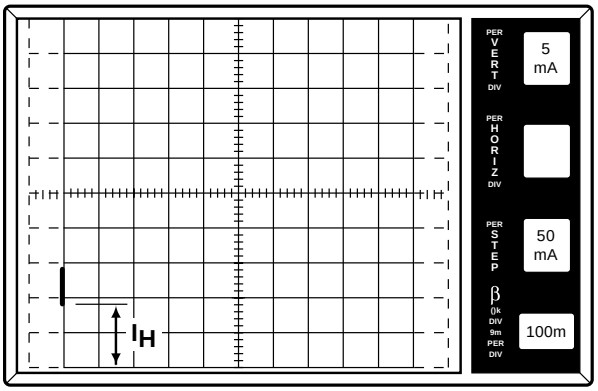


Figure AN1006.13 $I_{H\ (Forward)}$ = 8.2 mA

Procedure 9: $I_{H(Reverse)}$

To measure the $I_{H\ (Reverse)}$ parameter:

1. Set **Polarity** to (–).
2. Repeat Procedure 7 measuring $I_{H(Reverse)}$. (Read measurements from upper right corner of the screen.)

Procedure 10: I_{GT}

To measure the I_{GT} parameter:

1. Set **Polarity** to (+).
2. Set **Number of Steps** to *1*. (Set number of steps to *0* (zero) on 370.)
3. Set **Offset** by depressing *Aid*. (On 577, also set **Zero** button to *Offset*. Button is extended.)
4. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and *Oppose* at same time on 370.)
5. Set **Terminal Selector** to *Step Generator-Emitter Grounded*.
6. Set **Mode** to *Norm.*
7. Set **Max Peak Volts** to *15 V.* (*16 V* on 370)
8. Set **Power Dissipation** to *10 W.*
9. Set **Step Family** by depressing *Single*.
10. Set **Horizontal** knob to *2 V/DIV.*
11. Set **Vertical** knob to *50 mA/DIV.*
12. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).
13. Set **Variable Collector Supply Voltage** until voltage reaches 12 V on CRT.
14. After 12 V setting is completed, change **Horizontal** knob to *Step Generator*.

Procedure 11: I_{GT} – Quadrant I [MT2 (+) Gate (+)]

To measure the I_{GT} – Quadrant I parameter:

1. Set **Step/Offset Amplitude** to approximately 10% of rated I_{GT}.
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Gradually increase **Offset Multiplier** until device reaches conduction point. (Figure AN1006.14) Measure I_{GT} by following horizontal axis to the point where the vertical line passes through the axis. This measured value is I_{GT}. (On 370, I_{GT} is numerically displayed on screen under offset value.)

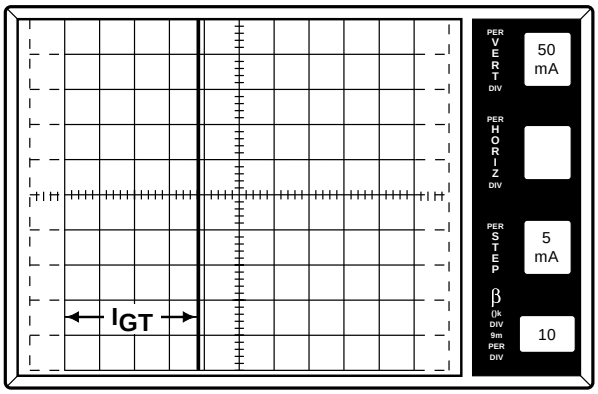


Figure AN1006.14 I_{GT} in Quadrant I = 18.8 mA

Procedure 12: I_{GT} – Quadrant II [MT2 (+) Gate (-)]

To measure the I_{GT} – Quadrant II parameter:

1. Set **Step/Offside Polarity** by depressing Invert (release button on 577).
2. Set **Polarity** to (+).
3. Set observed dot to bottom right corner of CRT grid by turning the horizontal position knob. When Quadrant II testing is complete, return dot to original position.
4. Repeat Procedure 11.

Procedure 13: I_{GT} – Quadrant III [MT2 (-) Gate (-)]

To measure the I_{GT} – Quadrant III parameter:

1. Set **Polarity** to (–).
2. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).
3. Repeat Procedure 11. (Figure AN1006.15)

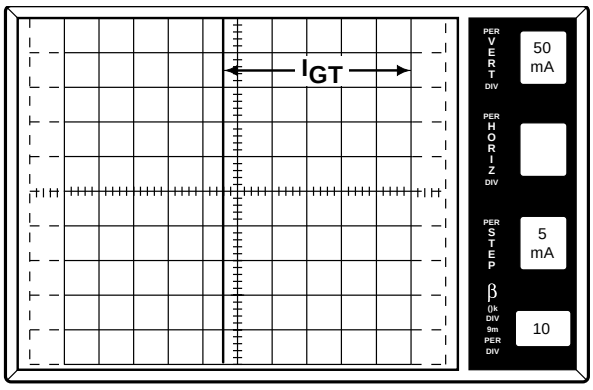


Figure AN1006.15 I_{GT} in Quadrant III = 27 mA

Procedure 14: I_{GT} – Quadrant IV [MT2 (-) Gate (+)]

To measure the I_{GT} – Quadrant IV parameter:

1. Set **Polarity** to (–).
2. Set **Step/Offset Polarity** by depressing *Invert* (release button on 577).
3. Set observed dot to top left corner of CRT grid by turning the **Horizontal** position knob. When Quadrant IV testing is complete, return dot to original position.
4. Repeat Procedure 11.

Procedure 15: V_{GT}

To measure the V_{GT} parameter:

1. Set **Polarity** to (+).
2. Set **Number of Steps** to *1*. (Set steps to *0* (zero) on 370.)
3. Set **Offset** by depressing *Aid*. (On 577, also set *0* (zero) button to *Offset*. Button is extended.)
4. Set **Offset Multiplier** to *0* (zero). (Press *Aid* and O*ppose* at same time on 370.)
5. Set **Terminal Selector** to *Step Generator-Emitter Grounded*.
6. Set **Mode** to *Norm*.
7. Set **Max Peak Volts** to *15 V*. (*16 V* on 370)
8. Set **Power Dissipation** to *10 W*.
9. Set **Step Family** by depressing *Single*.
10. Set **Horizontal** knob to *2 V/DIV*.
11. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).
12. Set **Current Limit** to 500 mA (not available on 577).
13. Increase **Variable Collector Supply Voltage** until voltage reaches 12 V on CRT.
14. After 12 V setting is complete, change **Horizontal** knob to *Step Generator.*

Procedure 16: V_{GT} – Quadrant I [MT2 (+) Gate (+)]

To measure the V_{GT} – Quadrant I parameter:

1. Set **Step/Offset Amplitude** to 20% of rated V_{GT}.
2. Set **Left-Right Terminal Jack Selector** to correspond with location of test fixture.
3. Gradually increase **Offset Multiplier** until device reaches conduction point. (Figure AN1006.16) Measure V_{GT} by following horizontal axis to the point where the vertical line passes through the axis. This measured value will be V_{GT}. (On 370, V_{GT} will be numerically displayed on screen under offset value.)

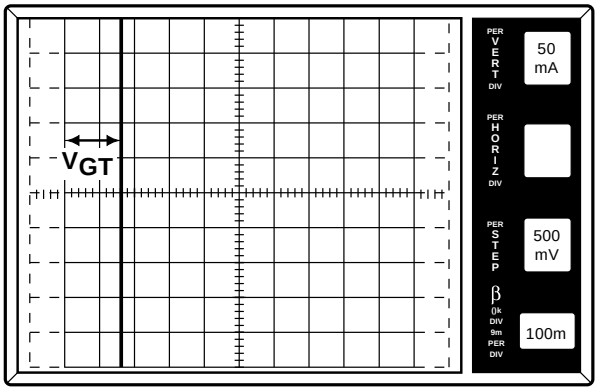


Figure AN1006.16 V_{GT} in Quadrant I = 780 mV

Procedure 17: V_{GT} – Quadrant II [MT2 (+) Gate (-)]

To measure the V_{GT} – Quadrant II parameter:

1. Set **Step/Offset Polarity** by depressing *Invert* (release button on 577).
2. Set **Polarity** to (+).
3. Set observed dot to bottom right corner of CRT grid by turning the horizontal position knob. When Quadrant II testing is complete, return dot to original position.
4. Repeat Procedure 16.

Procedure 18: V_{GT} – Quadrant III [MT2 (-) Gate (-)]

To measure the V_{GT} – Quadrant III parameter:

1. Set **Polarity** to (–).
2. Set **Step/Offset Polarity** to non-inverted position (button extended, on 577 button depressed).

3. Repeat Procedure 16. (Figure AN1006.17)

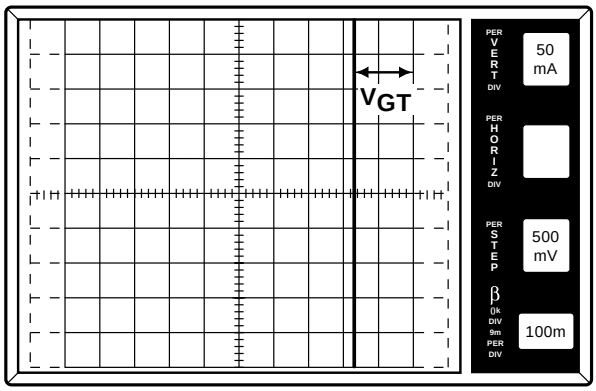


Figure AN1006.17 V_{GT} in Quadrant III = 820 mV

Procedure 19: V_{GT} – Quadrant IV [MT2 (-) Gate (+)]

To measure the V_{GT} – Quadrant IV parameter:

1. Set **Polarity** to (–).
2. Set **Step/Offset Polarity** by depressing *Invert* (release button on 577).
3. Set observed dot to top left corner of CRT grid by turning the **Horizontal** position knob. When testing is complete in Quadrant IV, return dot to original position.
4. Repeat Procedure 16.

Quadracs

Quadracs are simply triacs with an internally-mounted diac. As with triacs, *Quadracs* are bidirectional AC switches which are gate controlled for either polarity of main terminal voltage.

To connect the *Quadrac*:

1. Connect *Trigger* to *Base Terminal* (B).
2. Connect *MT1* to *Emitter Terminal* (E).
3. Connect *MT2* to *Collector Terminal* (C).

To begin testing, perform the following procedures.

Procedure 1: (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, (-)I_{DRM}

Note: The (+) and (-) symbols are used to designate the polarity of MT2 with reference to MT1.

To measure the (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, and (-)I_{DRM} parameter:

1. Set **Variable Collector Supply Voltage Range** to appropriate *Max Peak Volts* for device under test. (Value selected should be equal to or greater than the device's V_{DRM} rating).
2. Set **Horizontal** knob to sufficient scale to allow v*iewing of trace at the required voltage level. (The* 100 V/DIV scale should be used for testing devices having a V_{DRM} rating of 600 V or greater; the *50 V/DIV* scale for testing parts rated from 300 V to 500 V, and so on).
3. Set **Mode** to *Leakage*.
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base.*
7. Set **Vertical** knob to ten times the maximum leakage current (I_{DRM}) specified for the device.

   Note: The CRT readout should show 1% of the maximum leakage current. The vertical scale is divided by 1,000 when the leakage mode is used.

Procedure 2: (+)V_{DRM} and (+)I_{DRM}

To measure the (+)V_{DRM} and (+)I_{DRM} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Increase **Variable Collector Supply Voltage** to the rated V_{DRM} of the device and observe the dot on the CRT. (Read across horizontally from the dot to the vertical current scale.) This measured value is the leakage current. (Figure AN1006.18)

WARNING: Do NOT exceed V_{DRM}/V_{RRM} rating of SCRs, triacs, or *Quadracs*. These devices can be damaged.

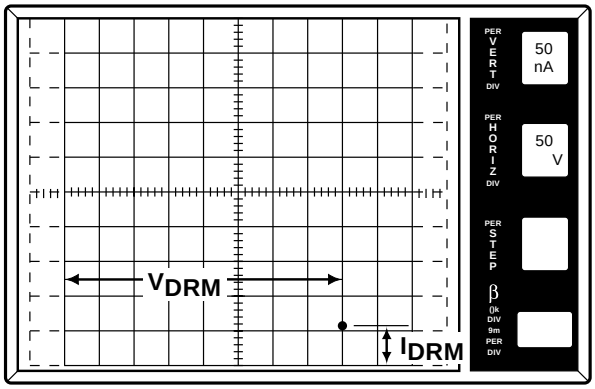


Figure AN1006.18 (+)I_{DRM} = 51 nA at (+)V_{DRM} = 400 V

Procedure 3: (-)V_{DRM} and (-)I_{DRM}

To measure the (-)V_{DRM} and (-)I_{DRM} parameter:

1. Set **Polarity** to (–).
2. Repeat Procedures 1 and 2. (Read measurements from upper right corner of screen).

Procedure 4: V_{BO}, I_{BO}, ΔV_{BO} (*Quadrac* Trigger Diac or Discrete Diac)

To connect the *Quadrac*:

1. Connect *MT1* to *Emitter Terminal* (E).
2. Connect *MT2* to *Collector Terminal* (C).
3. Connect *Trigger Terminal* to *MT2 Terminal* through a 10 Ω resistor.

To measure the V_{BO}, I_{BO}, and ΔV_{BO} parameter:

1. Set **Variable Collector Supply Voltage Range** to *75 Max Peak Volts.*(*80 V* on 370)
2. Set **Horizontal** knob to *10 V/DIV.*
3. Set **Vertical** knob to *50 µA/DIV.*
4. Set **Polarity** to *AC*.
5. Set **Mode** to *Norm*.
6. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)

7. Set **Terminal Selector** to *Emitter Grounded-Open Base*.

Procedure 5: V_{BO} (Positive and Negative)

To measure the $V_{BO\ (Positive\ and\ Negative)}$ parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Set **Variable Collector Supply Voltage** to *55 V* (*65 V* on 370) and apply voltage to the device under test (D.U.T.) using the **Left Hand Selector Switch.** The peak voltage at which current begins to flow is the V_{BO} value. (Figure AN1006.19)

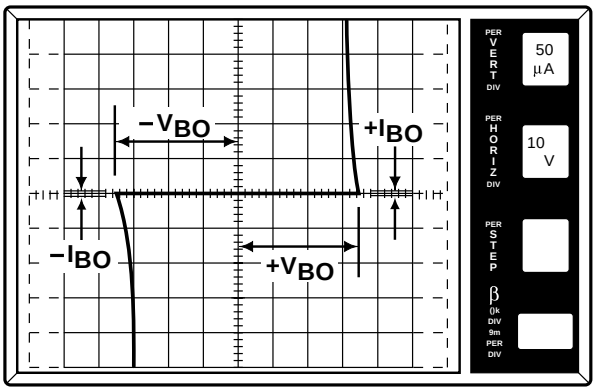


Figure AN1006.19 (+)V_{BO} = 35 V; (-)V_{BO} = 36 V; (±)I_{BO} < 10 A

Procedure 6: I_{BO} (Positive and Negative)

To measure the $I_{BO\ (Positive\ and\ Negative)}$ parameter, at the V_{BO} point, measure the amount of device current just before the device reaches the breakover point. The measured current at this point is the I_{BO} value.

Note: If I_{BO} is less than 10 µA, the current cannot readily be seen on curve tracer.

Procedure 7: ΔV_{BO} (Voltage Breakover Symmetry)

To measure the $\Delta V_{BO\ (Voltage\ Breakover\ Symmetry)}$ parameter:

1. Measure positive and negative V_{BO} values per Procedure 5.
2. Subtract the absolute value of V_{BO} (-) from V_{BO} (+).

   The absolute value of the result is:

   $\Delta V_{BO} = [\ |+V_{BO}| - |-V_{BO}|\ ]$

Procedure 8: V_{TM} (Forward and Reverse)

To test V_{TM}, the *Quadrac* must be connected the same as when testing V_{BO}, I_{BO}, and ΔV_{BO}.

To connect the *Quadrac*:

1. Connect *MT1* to *Emitter Terminal* (E).
2. Connect *MT2* to *Collector Terminal* (C).
3. Connect *Trigger Terminal* to *MT2 Terminal* through a 10 Ω resistor.

Note the following:

- Due to the excessive amount of power that can be generated in this test, only parts with an $I_{T(RMS)}$ rating of 8 A or less should be tested on standard curve tracer. If testing devices above 8 A, a Tektronix model 176 high-current module is required.
- A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin connections.

To measure the $V_{TM\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
2. Set **Max Peak Volts** to *75 V.* (*80 V* on 370)
3. Set **Mode** to *Norm*.
4. Set **Horizontal** knob to *0.5 V/DIV.*
5. Set **Power Dissipation** to *220 watts* (*100 watts* on a 577).
6. Set **Vertical** knob to a sufficient setting to allow the viewing of 1.4 times the $I_{T(RMS)}$ rating of the device $I_{T(peak)}$ on the CRT.

Procedure 9: $V_{TM(Forward)}$

To measure the $V_{TM\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$, which is 1.4 times the $I_{T(RMS)}$ rating of the triac under test.

Note: Model 370 current is limited to 10 A.

WARNING: Limit test time to 15 seconds maximum.

4. To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. This horizontal distance is the V_{TM} value. (Figure AN1006.20)

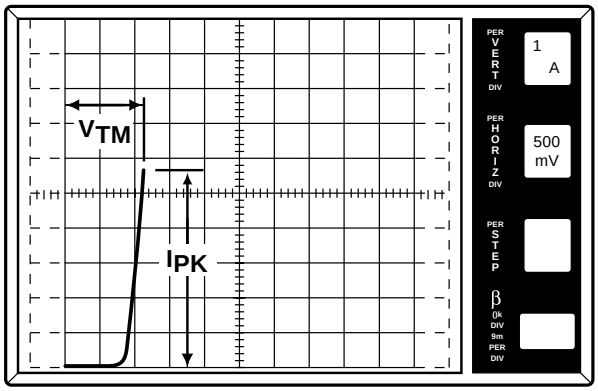


Figure AN1006.20 $V_{TM\ (Forward)}$ = 1.1 V at I_{PK} = 5.6 A

Procedure 10: $V_{TM(Reverse)}$

To measure the $V_{TM\ (Reverse)}$ parameter:

1. Set **Polarity** to (–).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$.
4. Measure $V_{TM(Reverse)}$ the same as in Procedure 8. (Read measurements from upper right corner of screen).

Procedure 11: $I_{H(Forward\ and\ Reverse)}$

For these steps, it is again necessary to connect the *Trigger* to *MT2* through a 10 Ω resistor. The other connections remain the same.

To measure the $I_{H\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Power Dissipation** to *50 W.*
2. Set **Max Peak Volts** to *75 V.* (*80 V* on 370)
3. Set **Mode** to *DC*.
4. Set **Horizontal** knob to *5 V/DIV.*
5. Set **Vertical** knob to approximately 10% of the maximum I_H specified.

   Note: Due to large variations of holding current values, the scale may have to be adjusted to observe holding current.
6. Set **Terminal Selector** to *Emitter Grounded-Open Base.*

Procedure 12: $I_{H(Forward)}$

To measure the $I_{H\ (Forward)}$ parameter:

1. Set **Polarity** to (+).
2. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
3. Increase **Variable Collector Supply Voltage** to maximum position (*100*).

   Note: Depending on the vertical scale being used, the dot may disappear completely from the screen.
4. Decrease **Variable Collector Supply Voltage** to the point where the line on the CRT changes to a dot. The position of the beginning point of the line, just before the line changes to a dot, represents the I_H value. (Figure AN1006.21)

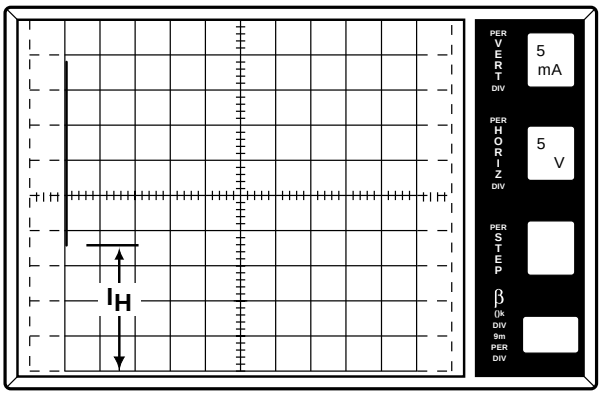


Figure AN1006.21 $I_{H\ (Forward)}$ = 18 mA

Procedure 13: $I_{H(Reverse)}$

To measure the $I_{H\ (Reverse)}$ parameter:

1. Set **Polarity** to (–).
2. Continue testing per Procedure 12 for measuring $I_{H\ (Reverse)}$.

Sidacs

The sidac is a bidirectional voltage-triggered switch. Upon application of a voltage exceeding the sidac breakover voltage point, the sidac switches on through a negative resistance region (similar to a diac) to a low on-state voltage. Conduction continues until current is interrupted or drops below minimum required holding current.

To connect the sidac:

1. Connect *MT1* to the *Emitter Terminal* (E).
2. Connect *MT2* to the *Collector Terminal* (C).

To begin testing, perform the following procedures.

Procedure 1: (+) V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, (-)I_{DRM}

Note: The (+) and (-) symbols are used to designate the polarity of MT2 with reference to MT1.

To measure the (+)V_{DRM}, (+)I_{DRM}, (-)V_{DRM}, and (-)I_{DRM} parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 Max Peak Volts*.
2. Set **Horizontal** knob to *50 V/DIV.*
3. Set **Mode** to *Leakage*.
4. Set **Polarity** to (+).
5. Set **Power Dissipation** to *2.2 W.* (*2 W* on 370)
6. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
7. Set **Vertical** knob to *50 µA/DIV.* (Due to leakage mode, the CRT readout will show 50 nA.)

Procedure 2: (+)V_{DRM} and (+)I_{DRM}

To measure the (+)V_{DRM} and (+)I_{DRM} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Increase **Variable Collector Supply Voltage** to the rated V_{DRM} of the device and observe the dot on the CRT. Read across horizontally from the dot to the vertical current scale. This measured value is the leakage current. (Figure AN1006.22)

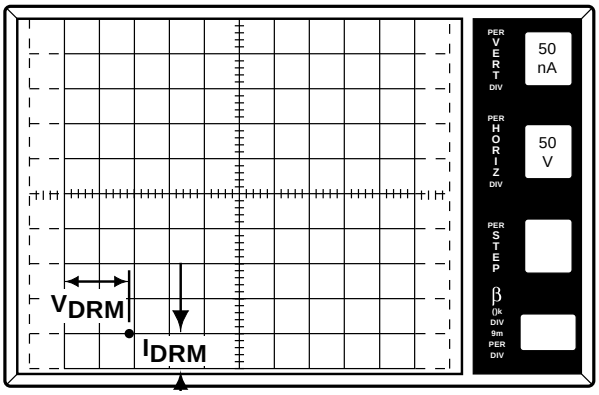


Figure AN1006.22 I_{DRM} = 50 nA at V_{DRM} = 90 V

Procedure 3: (-) V_{DRM} and (-) I_{DRM}

To measure the (-)V_{DRM} and (-)I_{DRM} parameter:

1. Set **Polarity** to (–).
2. Repeat Procedures 1 and 2. (Read measurements from upper right corner of the screen).

Procedure 4: V_{BO} and I_{BO}

To measure the V_{BO} and I_{BO} parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 Max Peak Volts.* (*2000 V* on 370)
2. Set **Horizontal** knob to a sufficient scale to allow viewing of trace at the required voltage level (***50 V/DIV*** for 95 V to 215 V V_{BO} range devices and ***100 V/DIV*** for devices having $V_{BO} \geq 15$ V).
3. Set **Vertical** knob to *50 µA/DIV.*
4. Set **Polarity** to *AC.*
5. Set **Mode** to *Norm*.
6. Set **Power Dissipation** to *10 W.*
7. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
8. Set ***Left-Right Terminal Jack Selector*** to correspond with location of test fixture.

Procedure 5: V_{BO}

To measure the V_{BO} parameter, increase **Variable Collector Supply Voltage** until breakover occurs. (Figure AN1006.23) The voltage at which current begins to flow and voltage on CRT does not increase is the V_{BO} value.

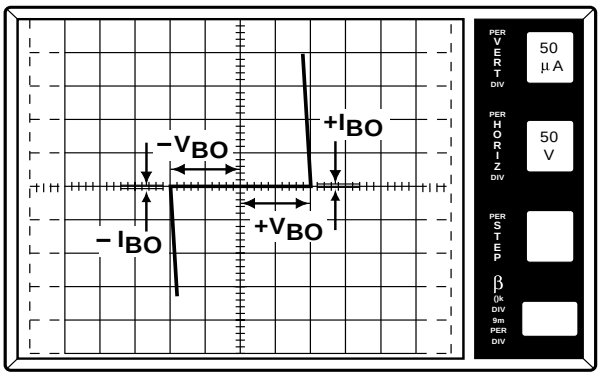


Figure AN1006.23 (+)V_{BO} = 100 V; (-)V_{BO} = 100 V; (±)I_{BO} < 10 µA

Procedure 6: I_{BO}

To measure the I_{BO} parameter, at the V_{BO} point, measure the amount of device current just before the device reaches the breakover mode. The measured current at this point is the I_{BO} value.

Note: If I_{BO} is less than 10 µA, the current cannot readily be seen on the curve tracer.

Procedure 7: $I_{H(Forward\ and\ Reverse)}$

To measure the $I_{H\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Variable Collector Supply Voltage Range** to *1500 Max Peak Volts* (*400 V* on 577; *2000 V* on 370).
2. Set **Horizontal** knob to a sufficient scale to allow viewing of trace at the required voltage level (*50 V/DIV* for devices with V_{BO} range from 95 V to 215 V and *100 V/DIV* for devices having $V_{BO} \geq 215$ V).
3. Set **Vertical** knob to 20% of maximum holding current specified.
4. Set **Polarity** to *AC.*
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *220 W* (*100 W* on 577).
7. Set **Terminal Selector** to *Emitter Grounded-Open Base*.
8. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.

   WARNING: Limit test time to 15 seconds maximum.
9. Increase **Variable Collector Supply Voltage** until device breaks over and turns on. (Figure AN1006.24)

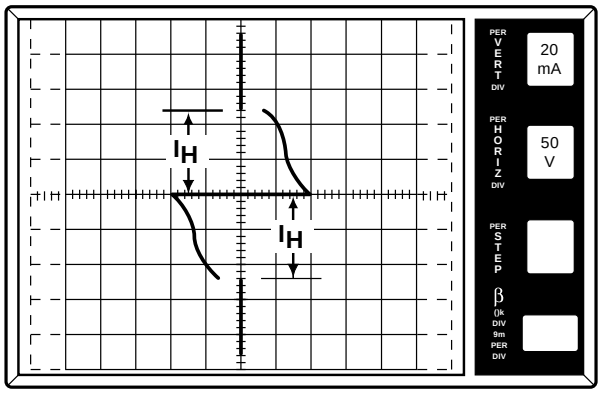


Figure AN1006.24 I_H = 48 mA in both forward and reverse directions

I_H is the vertical distance between the center horizontal axis and the beginning of the line located on center vertical axis.

Procedure 8: $V_{TM(Forward\ and\ Reverse)}$

To measure the $V_{TM\ (Forward\ and\ Reverse)}$ parameter:

1. Set **Variable Collector Supply Voltage Range** to *350 Max Peak Volts.* (*400 V* on 370)
2. Set **Horizontal** knob to *0.5 V/DIV.*
3. Set **Vertical** knob to *0.5 A/DIV.*
4. Set **Polarity** to (+).
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *220 W* (*100 W* on 577).
7. Set **Terminal Selector** to *Emitter Grounded-Open Base*.

Before continuing with testing, note the following:

- A Kelvin test fixture is required for this test. If a Kelvin fixture is not used, an error in measurement of V_{TM} will result due to voltage drop in fixture. If a Kelvin fixture is not available, Figure AN1006.3 shows necessary information to wire a test fixture with Kelvin Connections.

To continue testing, perform the following procedures.

Procedure 9: $V_{TM(Forward)}$

To measure the $V_{TM\ (Forward)}$ parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Increase **Variable Collector Supply Voltage** until current reaches rated $I_{T(peak)}$, which is 1.4 times the $I_{T(RMS)}$ rating of the sidac.

Note: Model 370 current is limited. Set to 400 mA. Check for 1.1 V MAX.

WARNING: Limit test time to 15 seconds.

3. To measure V_{TM}, follow along horizontal scale to the point where the trace crosses the $I_{T(peak)}$ value. This horizontal distance is the V_{TM} value. (Figure AN1006.25)

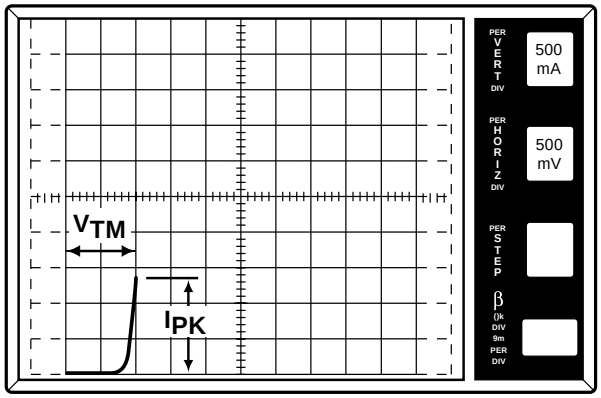


Figure AN1006.25 $V_{TM\ (Forward)}$ = 950 mV at I_{PK} = 1.4 A

Procedure 10: $V_{TM(Reverse)}$

To measure the $V_{TM\ (Reverse)}$ parameter:

1. Set **Polarity** to (–).
2. Repeat Procedure 8 to measure $V_{TM(Reverse)}$.

Diacs

Diacs are voltage breakdown switches used to trigger-on triacs and non-sensitive SCRs in phase control circuits.

Note: Diacs are bi-directional devices and can be connected in either direction.

To connect the diac:

1. Connect one side of the diac to the *Collector Terminal* (C).
2. Connect other side of the diac to the *Emitter Terminal* (E).

To begin testing, perform the following procedures.

Procedure 1: Curve Tracer Setup

To set the curve tracer and begin testing:

1. Set **Variable Collector Supply Voltage Range** to *75 Max Peak Volts.* (*80 V* on 370)
2. Set **Horizontal** knob to sufficient scale to allow viewing of trace at the required voltage level (*10 V to 20 V/DIV* depending on device being tested).
3. Set **Vertical** knob to *50 µA/DIV.*
4. Set **Polarity** to *AC.*
5. Set **Mode** to *Norm.*
6. Set **Power Dissipation** to *0.5 W.* (*0.4 W* on 370)
7. Set **Terminal Selector** to *Emitter Grounded-Open Base.*

Procedure 2: V_{BO}

To measure the V_{BO} parameter:

1. Set **Left-Right Terminal Jack Selector** to correspond with the location of the test fixture.
2. Set **Variable Collector Supply Voltage** to *55 V* (*65 V* for 370) and apply voltage to device under test (D.U.T.), using **Left-Right-Selector Switch**. The peak voltage at which current begins to flow is the V_{BO} value. (Figure AN1006.26)

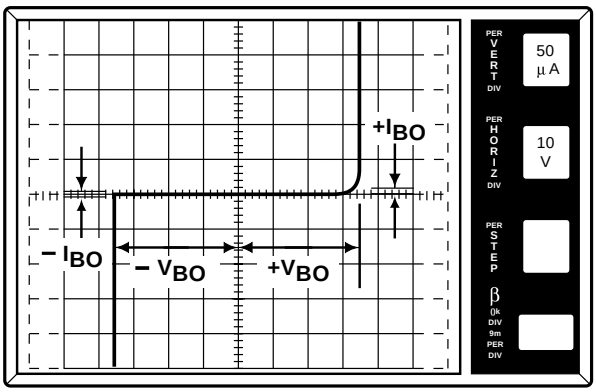


Figure AN1006.26 (+)V_{BO} = 35 V; (-)V_{BO} = 36 V; (±)I_{BO} < 15 µA; (-)I_{BO} < 10 µA and Cannot Be Read Easily

Procedure 3: I_{BO}

To measure the I_{BO} parameter, at the V_{BO} point, measure the amount of device current just before the device reaches the breakover mode. The measured current at this point is the I_{BO} value.

Note: If I_{BO} is less than 10 µA, the current cannot readily be seen on the curve tracer.

Procedure 4: $\Delta V_{BO(Voltage\ Breakover\ Symmetry)}$

To measure the $\Delta V_{BO\ (Voltage\ Breakover\ Symmetry)}$ parameter:

1. Measure positive and negative values of V_{BO} as shown in Figure AN1006.26.
2. Subtract the absolute value of $V_{BO}(-)$ from $V_{BO}(+)$.

   The absolute value of the result is:

   $\Delta V_{BO} = [\ |+V_{BO}| - |-V_{BO}|\ ]$

Model 370 Curve Tracer Procedure Notes

Because the curve tracer procedures in this application note are written for the Tektronix model 576 curve tracer, certain settings must be adjusted when using model 370. Variable Collector Supply Voltage Range and Power Dissipation controls have different scales than model 576. The following table shows the guidelines for setting Power Dissipation when using model 370. (Figure AN1006.27)

Model 576	Model 370
If power dissipation is 0.1 W,	set at 0.08 W.
If power dissipation is 0.5 W,	set at 0.4 W.
If power dissipation is 2.2 W,	set at 2 W.
If power dissipation is 10 W,	set at 10 W.
If power dissipation is 50 W,	set at 50 W.
If power dissipation is 220 W,	set at 220 W.

Although the maximum power setting on the model 370 curve tracer is 200 W, the maximum collector voltage available is only 400 V at 220 W. The following table shows the guidelines for adapting Collector Supply Voltage Range settings for model 370 curve tracer procedures:

Model 576	Model 370
If voltage range is 15 V,	set at 16 V.
If voltage range is 75 V,	set at 80 V.
If voltage range is 350 V,	set at 400 V.
If voltage range is 1500 V,	set at 2000 V.

The following table shows the guidelines for adapting terminal selector knob settings for model 370 curve tracer procedures:

Model 576	Model 370
If Step generator (base) is emitter grounded,	then Base Step generator is emitter common.
If Emitter grounded is open base,	then Base open is emitter common.

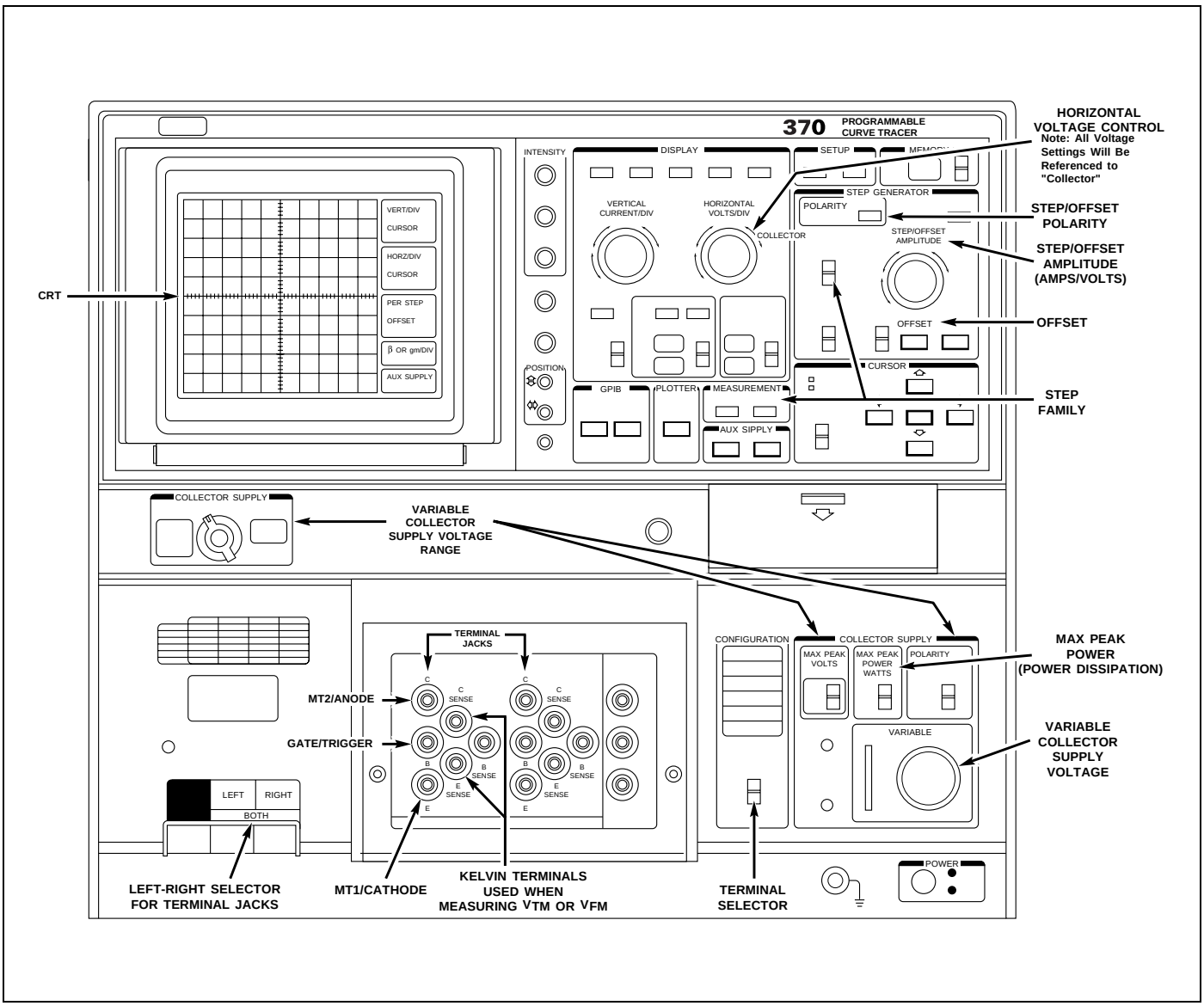


Figure AN1006.27 Tektronix Model 370 Curve Tracer

Model 577 Curve Tracer Procedure Notes

Because the curve tracer procedures in this application note are written for the Tektronix model 576 curve tracer, certain settings must be adjusted when using model 577. Model 576 curve tracer has separate controls for polarity (AC,+,-) and mode (Norm, DC, Leakage), whereas Model 577 has only a polarity control. The following table shows the guidelines for setting Collector Supply Polarity when using model 577. (Figure AN1006.28)

Model 576	Model 577
If using Leakage mode along with polarity setting of +(NPN) and -(PNP), [vertical scale divided by 1,000],	set **Collector Supply Polarity** to either *+DC* or *-DC*, depending on polarity setting specified in the procedure. The vertical scale is read directly from the scale on the control knob.
If using DC mode along with either +(NPN) or -(PNP) polarity,	set **Collector Supply Polarity** to either *+DC* or *-DC* depending on polarity specified.
If using Norm mode along with either +(NPN) or -(PNP) polarity,	set **Collector Supply Polarity** to either *+(NPN)* or *-(PNP)* per specified procedure.
If using Norm mode with *AC* polarity,	set **Collector Supply Polarity** to *AC*.

One difference between models 576 and 577 is the Step/Offset Polarity setting. The polarity is inverted when the button is depressed on the Model 576 curve tracer. The Model 577 is opposite — the Step/Offset Polarity is “inverted” when the button is extended and “Normal” when the button is depressed. The Step/Offset Polarity is used only when measuring I_{GT} and V_{GT} of triacs and *Quadracs* in Quadrants I through IV.

Also, the Variable Collector Supply Voltage Range and Power Dissipation controls have different scales than model 576. The following table shows the guidelines for setting Power Dissipation when using model 577.

Model 576	Model 577
If power dissipation is 0.1 W,	set at 0.15 W.
If power dissipation is 0.5 W,	set at 0.6 W.
If power dissipation is 2.2 W,	set at 2.3 W.
If power dissipation is 10 W,	set at 9 W.
If power dissipation is 50 W,	set at 30 W.
If power dissipation is 220 W,	set at 100 W.

Although the maximum power setting on model 576 curve tracer is 220 W (compared to 100 W for model 577), the maximum collector current available is approximately the same. This is due to the minimum voltage range on model 577 curve tracer being 6.5 V compared to 15 V for model 576. The following table shows the guidelines for adapting Collector Voltage Supply Range settings for model 577 curve tracer procedures:

Model 576	Model 577
If voltage range is 15 V,	set at either 6.5 V or 25 V, depending on parameter being tested. Set at 6.5 V when measuring V_{TM} (to allow maximum collector current) and set at 25 V when measuring I_{GT} and V_{GT}.
If voltage range is 75 V,	set at 100 V.
If voltage range is 1500 V,	set at 1600 V.

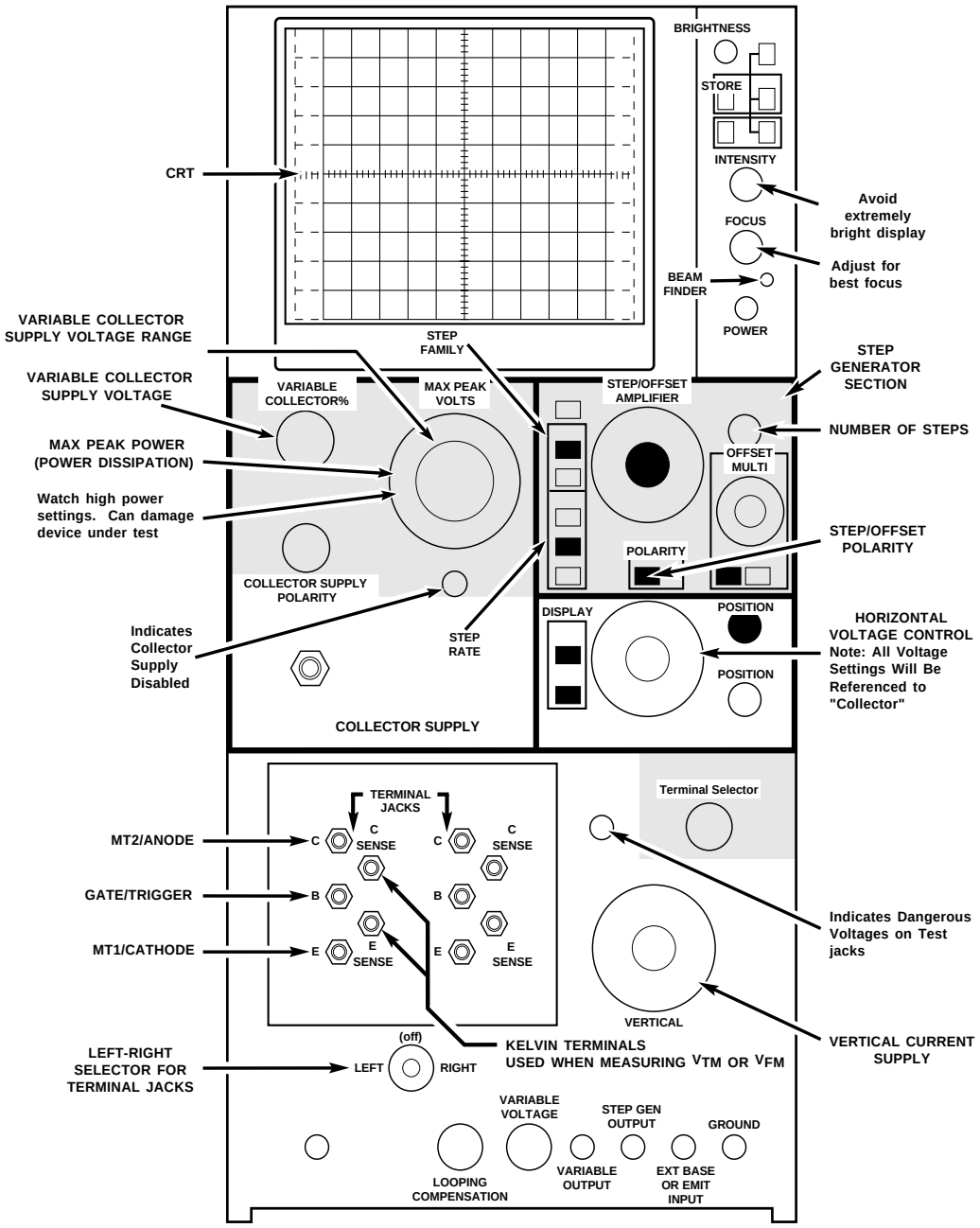


Figure AN1006.28 Tektronix Model 577 Curve Tracer

Notes

AN1007

Thyristors Used as AC Static Switches and Relays

Introduction

Since the SCR and the triac are bistable devices, one of their broad areas of application is in the realm of signal and power switching. This application note describes circuits in which these thyristors are used to perform simple switching functions of a general type that might also be performed non-statically by various mechanical and electromechanical switches. In these applications, the thyristors are used to open or close a circuit completely, as opposed to applications in which they are used to control the magnitude of average voltage or energy being delivered to a load. These latter types of applications are described in detail in “Phase Control Using Thyristors” (AN1003).

Static AC Switches

Normally Open Circuit

The circuit shown in Figure AN1007.1 provides random (anywhere in half-cycle), fast turn-on (<10 µs) of AC power loads and is ideal for applications with a high-duty cycle. It eliminates completely the contact sticking, bounce, and wear associated with conventional electromechanical relays, contactors, and so on. As a substitute for control relays, thyristors can overcome the differential problem; that is, the spread in current or voltage between pickup and dropout because thyristors effectively drop out every half cycle. Also, providing resistor R_1 is chosen correctly, the circuits are operable over a much wider voltage range than is a comparable relay. Resistor R_1 is provided to limit gate current (I_{GTM}) peaks. Its resistance plus any contact resistance (R_C) of the control device and load resistance (R_L) should be just greater than the peak supply voltage divided by the peak gate current rating of the triac. If R_1 is set too high, the triacs may not trigger at the beginning of each cycle, and phase control of the load will result with consequent loss of load voltage and waveform distortion. For inductive loads, an RC snubber circuit, as shown in Figure AN1007.1, is required. However, a snubber circuit is not required when an alternistor triac is used.

Figure AN1007.2 illustrates an analysis to better understand a typical static switch circuit. The circuit operation occurs when switch S_1 is closed, since the triac Q_1 will initially be in the blocking condition. Current flow will be through load R_L, S_1, R_1, and gate to MT1 junction of the thyristor. When this current reaches the required value of I_{GT}, the MT2 to MT1 junctions will switch to the conduction state and the voltage from MT2 to MT1 will be V_T. As the current approaches the zero crossing, the load current will fall below holding current turning the triac Q_1 device off until it is refired in the next half cycle. Figure AN1007.3 illustrates the voltage waveform appearing across the MT2 to MT1 terminals of Q_1. Note that the maximum peak value of current which S_1 will carry would be 25 mA since Q_1 has a 25 mA maximum I_{GT} rating. Additionally, no arcing of a current value greater than 25 mA when opening S_1 will occur when controlling an inductive load. It is important also to note that the triac Q_1 is operating in Quadrants I and III, the more sensitive and most suitable gating modes for triacs. The voltage rating of S_1 (mechanical switch or reed switch) must be equivalent to or greater than line voltage applied.

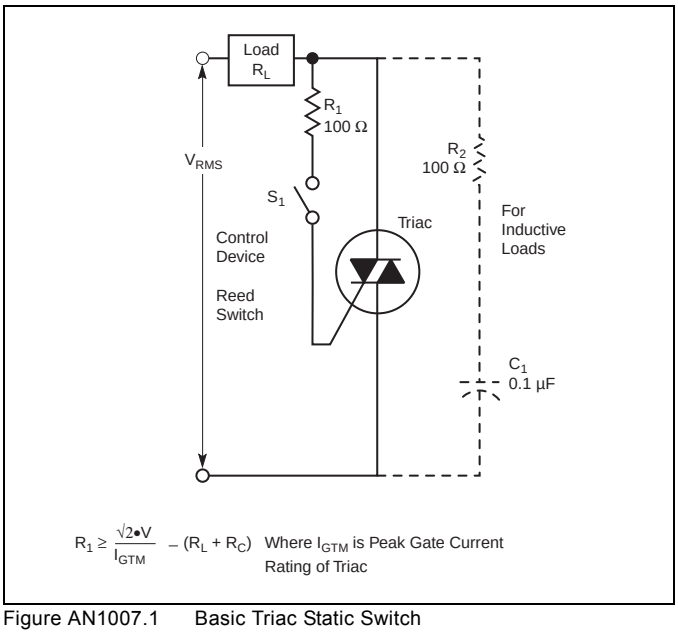


Figure AN1007.1 Basic Triac Static Switch

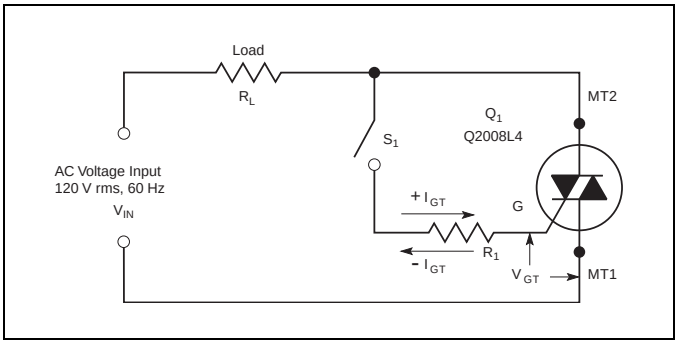


Figure AN1007.2 Analysis of Static Switch

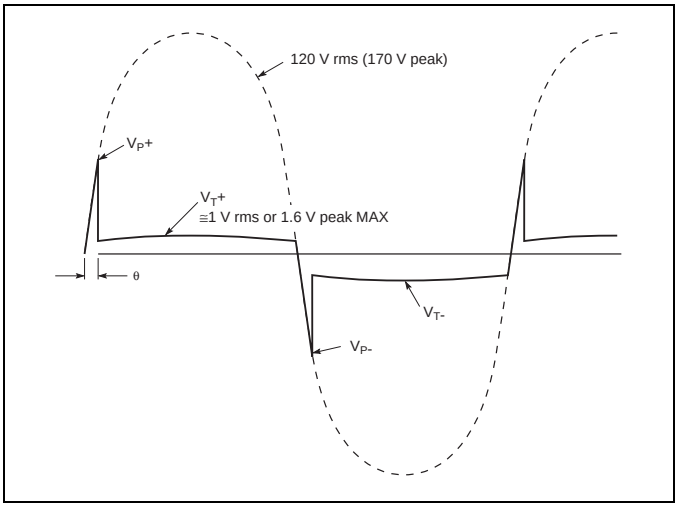


Figure AN1007.3 Waveform Across Static Switch

A typical example would be in the application of this type circuit for the control of 5 A resistive load with 120 V rms input voltage. Choosing a value of 100 Ω for R_1 and assuming a typical value of 1 V for the gate to MT1 (V_{GT}) voltage, we can solve for V_P by the following:

$$V_P = I_{GT} (R_L + R_1) + V_{GT}$$

Note: R_C is not included since it is negligible.

$$V_P = 0.025 (24 + 100) + 1.0 = 4.1 \text{ V}$$

Additionally the turn-on angle is

$$\theta = \text{Sin}^{-1} \frac{4.1}{170 V_{PK}} \quad [\theta = 1.4°]$$

The power lost by the turn-on angle is essentially zero. The power dissipation in the gate resistor is very minute. A 100 Ω, 0.25 W rated resistor may safely be used. The small turn-on angle also ensures that no appreciable RFI is generated.

The relay circuit shown in Figure AN1007.1 and Figure AN1007.2 has several advantages in that it eliminates contact bounce, noise, and additional power consumption by an energizing coil and can carry an in-rush current of many times its steady state rating.

The control device S_1 indicated can be either electrical or mechanical in nature. Light-dependent resistors and light- activated semiconductors, optocoupler, magnetic cores, and magnetic reed switches are all suitable control elements. Regardless of the switch type chosen, it must have a voltage rating equal to or greater than the peak line voltage applied. In particular, the use of hermetically sealed reed switches as control elements in combination with triacs offers many advantages. The reed switch can be actuated by passing DC current through a small coiled wire or by the proximity of a small magnet. In either case, complete electrical isolation exists between the control signal input, which may be derived from many sources, and the switched power output. Long life of the triac/reed switch combination is ensured by the minimal volt-ampere switching load placed on the reed switch by the triac triggering requirements. The thyristor ratings determine the amount of load power that can be switched.

Normally Closed Circuit

With a few additional components, the thyristor can provide a normally closed static switch function. The critical design portion of this static switch is a clamping device to turn off/eliminate gate drive and maintain very low power dissipation through the clamping component plus have low by-pass leakage around the power thyristor device. In selecting the power thyristor for load requirements, gate sensitivity becomes critical to maintain low power requirements. Either sensitive SCRs or sensitive logic triacs must be considered, which limits the load in current capacity and type. However, this can be broader if an extra stage of circuitry for gating is permitted.

Figure AN1007.4 illustrates an application using a normally closed circuit driving a sensitive SCR for a simple but precise temperature controller. The same basic principle could be applied to a water level controller for a motor or solenoid. Of course, SCR and diode selection would be changed depending on load current requirements.

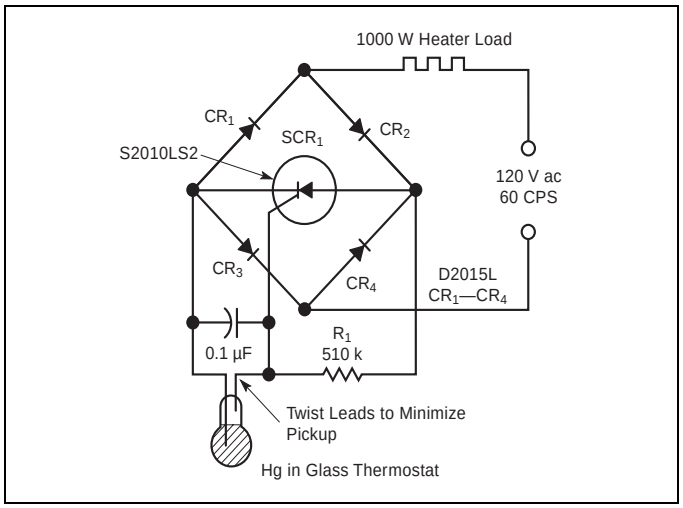


Figure AN1007.4 Normally Closed Temperature Controller

A mercury-in-glass thermostat is an extremely sensitive measuring instrument, capable of sensing changes in temperature as small as 0.1 °C. Its major limitation lies in its very low current-handling capability for reliability and long life, and contact current should be held below 1 mA. In the circuit of Figure AN1007.4, the S2010LS2 SCR serves as both current amplifier for the Hg thermostat and as the main load switching element.

With the thermostat open, the SCR will trigger each half cycle and deliver power to the heater load. When the thermostat closes, the SCR can no longer trigger and the heater shuts off. Maximum current through the thermostat in the closed position is less than 250 µA rms.

Figure AN1007.5 shows an all solid state, optocoupled, normally closed switch circuit. By using a low voltage SBS triggering device, this circuit can turn on with only a small delay in each half cycle and also keep gating power low. When the optocoupled transistor is turned on, the gate drive is removed with only a few milliamps of bypass current around the triac power device. Also, by use of the BS08D and 0.1 µF, less sensitive triacs and alternistors can be used to control various types of high current loads.

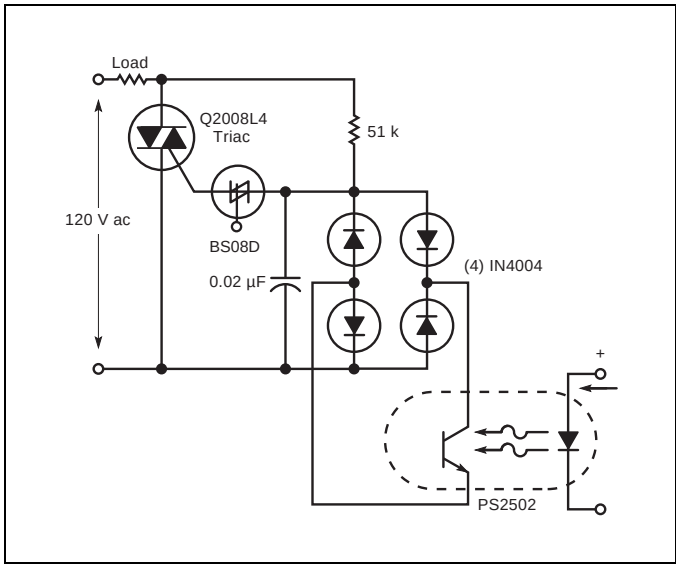


Figure AN1007.5 Normally Closed Switch Circuit

Optocoupled Driver Circuits

Random Turn-on, Normally Open

Many applications use optocouplers to drive thyristors. The combination of a good optocoupler and a triac or alternistor makes an excellent, inexpensive solid state relay. Application information provided by the optocoupler manufacturers is not always best for application of the power thyristor. Figure AN1007.6 shows a standard circuit for a resistive load.

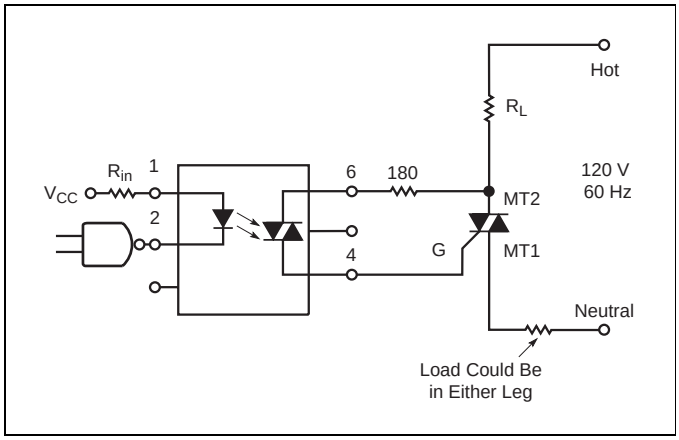


Figure AN1007.6 Optocoupled Circuit for Resistive Loads (Triac or Alternistor)

A common mistake in this circuit is to make the series gate resistor too large in value. A value of 180 Ω is shown in a typical application circuit by optocoupler manufacturers. The 180 Ω is based on limiting the current to 1 A peak at the peak of a 120 V line input for Fairchild and Toshiba optocoupler I_{TSM} rating. This is good for protection of the optocoupler output triac, as well as the gate of the power triac on a 120 V line; however, it must be lowered if a 24 V line is being controlled, or if the R_L (resistive load) is 200 W or less. This resistor limits current for worst case turn-on at the peak line voltage, but it also sets turn-on point (conduction angle) in the sine wave, since triac gate current is determined by this resistor and produced from the sine wave voltage as illustrated in Figure AN1007.2. The load resistance is also important, since it can also limit the amount of available triac gate current. A 100 Ω gate resistor would be a better choice in most 120 V applications with loads greater than 200 W and optocouplers from Quality Technologies or Vishay with optocoupler output triacs that can handle 1.7 A_{PK} (I_{TSM} rating) for a few microseconds at the peak of the line. For loads less than 200 W, the resistor can be dropped to 22 Ω. Remember that if the gate resistor is too large in value, the triac will not turn on at all or not turn on fully, which can cause excessive power dissipation in the gate resistor, causing it to burn out. Also, the voltage and dv/dt rating of the optocoupler's output device must be equal to or greater than the voltage and dv/dt rating of the triac or alternistor it is driving.

Figure AN1007.7 illustrates a circuit with a dv/dt snubber network included. This is a typical circuit presented by optocoupler manufacturers.

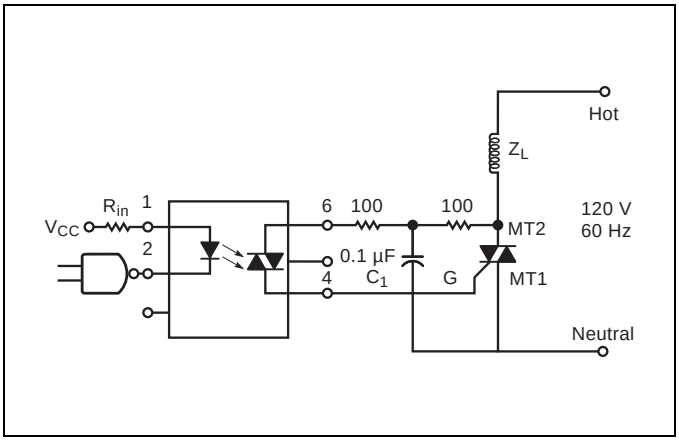


Figure AN1007.7 Optocoupler Circuit for Inductive Loads (Triac or Alternistor)

This “T” circuit hinges around one capacitor to increase dv/dt capability to either the optocoupler output triac or the power triac. The sum of the two resistors then forms the triac gate resistor.

Both resistors should then be standardized and lowered to 100 Ω. Again, this sum resistance needs to be low, allowing as much gate current as possible without exceeding the instantaneous current rating of the opto output triac or triac gate junction. By having 100 Ω for current limit in either direction from the capacitor, the optocoupler output triac and power triac can be protected against di/dt produced by the capacitor. Of course, it is most important that the capacitor be connected between proper terminals of triac. For example, if the capacitor and series resistor are accidentally connected between the gate and MT2, the triac will turn on from current produced by the capacitor, resulting in loss of control.

For low current (mA) and/or highly inductive loads, it may be necessary to have a latching network (3.3 kΩ + 0.047 µF) connected directly across the power triac. The circuit shown in Figure AN1007.8 illustrates the additional latching network.

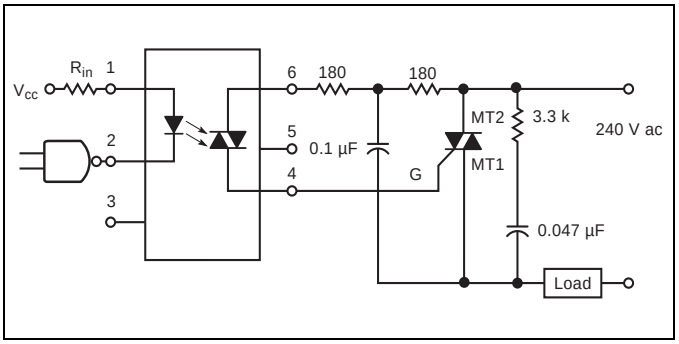


Figure AN1007.8 Optocoupler Circuit for Lower Current Inductive Loads (Triac or Alternistor)

In this circuit, the series gate resistors are increased to 180 Ω each, since a 240 V line is applied. Note that the load is placed on the MT1 side of the power triac to illustrate that load placement is **not** important for the circuit to function properly.

Also note that with standard U.S. residential 240 V home wiring, both sides of the line are hot with respect to ground (no neutral). Therefore, for some 240 V line applications, it will be necessary to have a triac switch circuit in both sides of the 240 V line input.

If an application requires back-to-back SCRs instead of a triac or alternistor, the circuit shown in Figure AN1007.9 may be used.

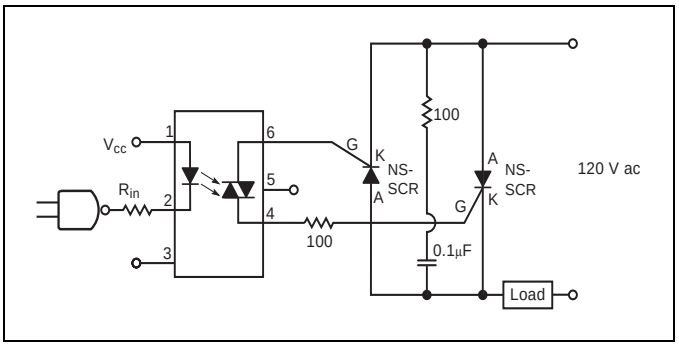


Figure AN1007.9 Optocoupled Circuit for Heavy-duty Inductive Loads

All application comments and recommendations for optocoupled switches apply to this circuit. However, the snubber network can be applied only across the SCRs as shown in the illustration. The optocoupler should be chosen for best noise immunity. Also, the voltage rating of the optocoupler output triac must be equal to or greater than the voltage rating of SCRs.

Summary of Random Turn-on Relays

As shown in Figure AN1007.10, if the voltage across the load is to be phase controlled, the input control circuitry must be synchronized to the line frequency and the trigger pulses delayed from zero crossing every half cycle. If the series gate resistor is chosen to limit the peak current through the opto-driver to less than 1 A, then on a 120 V ac line the peak voltage is 170 V; therefore, the resistor is 180 Ω. On a 240 V ac line the peak voltage is 340 V; therefore, the resistor should be 360 Ω. These gate pulses are only as long as the device takes to turn on (typically, 5 µs to 6 µs); therefore, 0.25 W resistor is adequate.

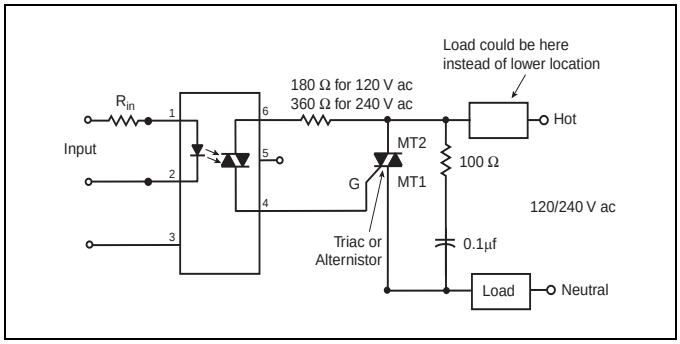


Figure AN1007.10 Random Turn-on Triac Driver

Select the triac for the voltage of the line being used, the current through the load, and the type of load. Since the peak voltage of a 120 V ac line is 170 V, you would choose a 200 V (MIN) device. If the application is used in an electrically noisy industrial environment, a 400 V device should be used. If the line voltage to be controlled is 240 V ac with a peak voltage of 340 V, then use at least a 400 V rated part or 600 V for more design margin. Selection of the voltage rating of the opto-driver must be the same or higher than the rating of the power triac. In electrically noisy industrial locations, the dv/dt rating of the opto-driver and the triac must be considered.

The RMS current through the load and main terminals of the triac should be approximately 70% of the maximum rating of the device. However, a 40 A triac should not be chosen to control a 1 A load due to low latching and holding current requirements. Remember that the case temperature of the triac must be maintained at or below the current versus temperature curve specified on its data sheet. As with all semiconductors the lower the case temperature the better the reliability. Opto-driven gates normally do not use a sensitive gate triac. The opto-driver can supply up to 1 A gate pulses and less sensitive gate triacs have better dv/dt capability. If the load is resistive, it is acceptable to use a standard triac. However, if the load is a heavy inductive type, then an alternistor triac, or back-to-back SCRs as shown in Figure AN1007.9, is recommended. A series RC snubber network may or may not be necessary when using an alternistor triac. Normally a snubber network is not needed when using an alternistor because of its high dv/dt and dv/dt(c) capabilities. However, latching network as described in Figure AN1007.8 may be needed for low current load variations.

Zero Crossing Turn-on, Normally Open Relay Circuits

When a power circuit is mechanically switched on and off mechanically, generated high-frequency components are generated that can cause interference problems such as RFI. When power is initially applied, a step function of voltage is applied to the circuit which causes a shock excitation. Random switch opening stops current off, again generating high frequencies. In addition, abrupt current interruption in an inductive circuit can lead to high induced-voltage transients.

The latching characteristics of thyristors are ideal for eliminating interference problems due to current interruption since these devices can only turn off when the on-state current approaches zero, regardless of load power factor.

On the other hand, interference-free turn-on with thyristors requires special trigger circuits. It has been proven experimen-

tally that general purpose AC circuits will generate minimum electromagnetic interference (EMI) if energized at zero voltage.

The ideal AC circuit switch, therefore, consists of a contact which closes at the instant when voltage across it is zero and opens at the instant when current through it is zero. This has become known as “zero-voltage switching.”

For applications that require synchronized zero-crossing turn-on, the illustration in Figure AN1007.11 shows a circuit which incorporates an optocoupler with a built-in zero-crossing detector

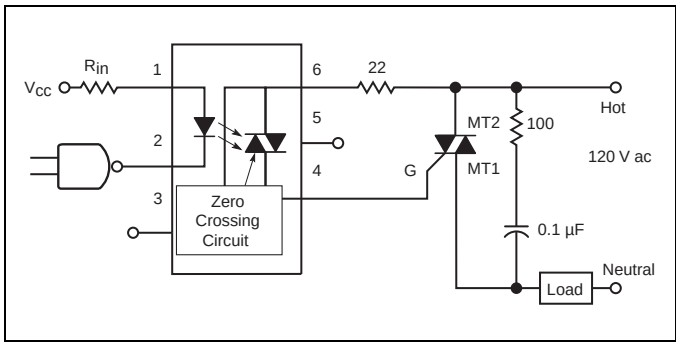


Figure AN1007.11 Optocoupled Circuit with Zero-crossing Turn-on (Triac or Alternistor)

Also, this circuit includes a dv/dt snubber network connected across the power triac. This typical circuit illustrates switching the hot line; however, the load may be connected to either the hot or neutral line. Also, note that the series gate resistor is low in value (22 Ω), which is possible on a 120 V line and above, since zero-crossing turn-on is ensured in any initial half cycle.

Summary of Zero Crossing Turn-on Circuits

Zero voltage crossing turn-on opto-drivers are designed to limit turn-on voltage to less than 20 V. This reduces the amount of RFI and EMI generated when the thyristor switches on. Because of this zero turn-on, these devices cannot be used to phase control loads. Therefore, speed control of a motor and dimming of a lamp cannot be accomplished with zero turn-on opto-couplers.

Since the voltage is limited to 20 V or less, the series gate resistor that limits the gate drive current has to be much lower with a zero crossing opto-driver. With typical inhibit voltage of 5 V, an alternistor triac gate could require a 160 mA at -30 °C (5 V/ 0.16 A = 31 Ω gate resistor). If the load has a high inrush current, then drive the gate of the triac with as much current as reliably possible but stay under the I_{TSM} rating of the opto-driver. By using 22 Ω for the gate resistor, a current of at least 227 mA is supplied with only 5 V, but limited to 909 mA if the voltage goes to 20 V. As shown in Figure AN1007.12, Figure AN1007.13, and Figure AN1007.14, a 22 Ω gate resistor is a good choice for various zero crossing controllers.

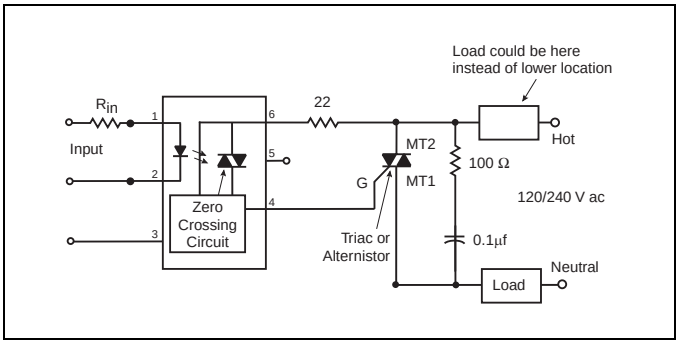


Figure AN1007.12 Zero Crossing Turn-on Opto Triac Driver

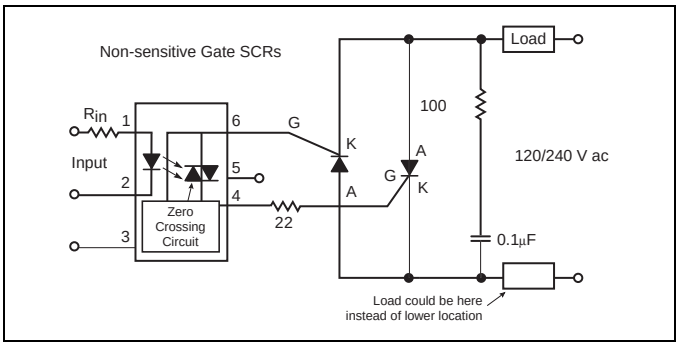


Figure AN1007.13 Zero Crossing Turn-on Non-sensitive SCR Driver

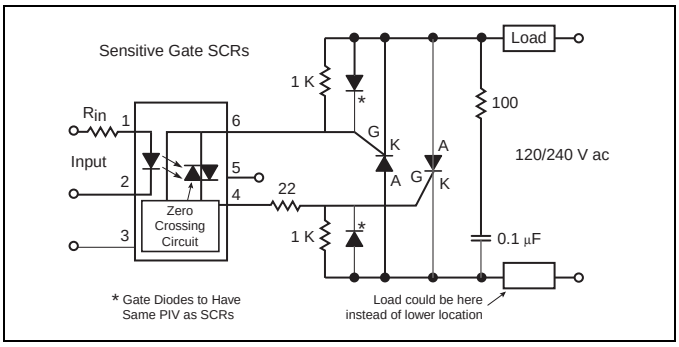


Figure AN1007.14 Zero Crossing Turn-on Opto-sensitive Gate SCR Driver

Time Delay Relay Circuit

By combining a 555 timer IC with a triac, various time delays of several seconds can be achieved for delayed activation of solid state relays or switches. Figure AN1007.15 shows a solid state timer delay relay using a sensitive gate triac and a 555 timer IC. The 555 timer precisely controls time delay of operation using an external resistor and capacitor, as illustrated by the resistor and capacitor combination curves. (Figure AN1007.16)

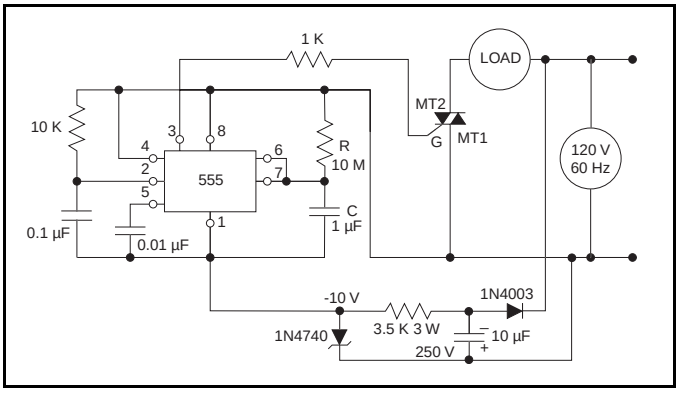


Figure AN1007.15 555 timer circuit with 10 second delay

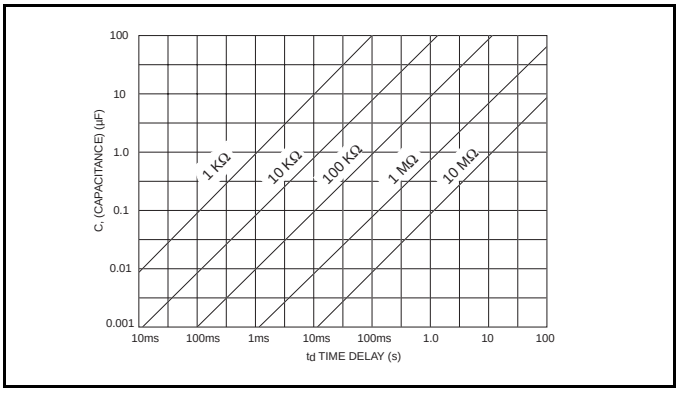


Figure AN1007.16 Resistor (R) and capacitor (C) combination curves

IR Motion Control

An example of a more complex triac switch is an infrared (IR) motion detector controller circuit. Some applications for this circuit are alarm systems, automatic lighting, and auto doorbells.

Figure AN1007.17 shows an easy- to-implement automatic lighting system using an infrared motion detector control circuit. A commercially available LSI circuit HT761XB, from *Holtek,* integrates most of the analog functions. This LSI chip, U2, contains the op amps, comparators, zero crossing detection, oscillators, and a triac output trigger. An external RC that is connected to the OSCD pin determines the output trigger pulse width. (*Holtek Semiconductor Inc.* is located at No.3, Creation Road II, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.) Device U1 provides the infrared sensing. Device R13 is a photo sensor that serves to prevent inadvertent triggering under daylight or other high light conditions.

Choosing the right triac depends on the load characteristics. For example, an incandescent lamp operating at 110 V requires a 200 V, 8 A triac. This gives sufficient margin to allow for the high current state during lamp burn out. U2 provides a minimum output triac negative gate trigger current of 40 mA, thus operating in QII & QIII. This meets the requirements of a 25 mA gate triac. *Teccor* also offers alternistor triacs for inductive load conditions.

This circuit has three operating modes (ON, AUTO, OFF), which can be set through the mode pin. While the LSI chip is working in the auto mode, the user can override it and switch to the test mode, or manual on mode, or return to the auto mode by switching the power switch. More information on this circuit, such as mask options for the infrared trigger pulse and flash options, are available in the *Holtek* HT761X General Purpose PIR Controller specifications.

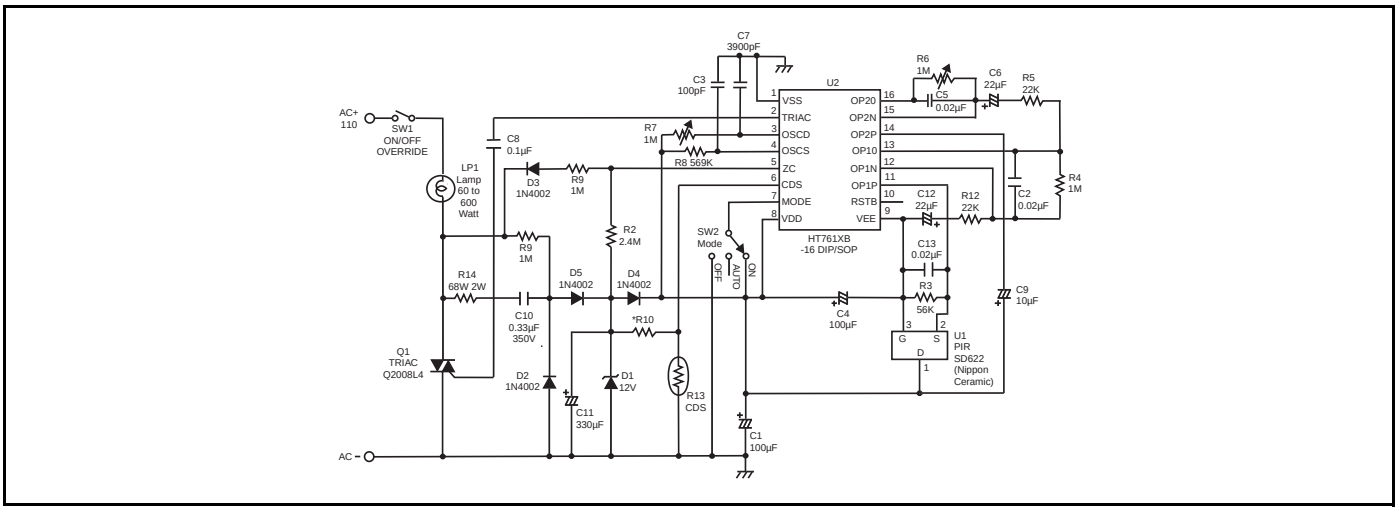


Figure AN1007.17 I R motion control circuit

AN1008

Explanation of Maximum Ratings and Characteristics for Thyristors

Introduction

Data sheets for SCRs and triacs give vital information regarding maximum ratings and characteristics of thyristors. If the **maximum ratings** of the thyristors are surpassed, possible irreversible damage may occur. The **characteristics** describe various pertinent device parameters which are guaranteed as either minimums or maximums. Some of these characteristics relate to the ratings but are not ratings in themselves. The characteristic does not define what the circuit must provide or be restricted to, but defines the device characteristic. For example, a minimum value is indicated for the dv/dt because this value depicts the guaranteed worst-case limit for all devices of the specific type. This minimum dv/dt value represents the maximum limit that the circuit should allow.

Maximum Ratings

V_{RRM}: Peak Repetitive Reverse Voltage — SCR

The peak repetitive reverse voltage rating is the maximum peak reverse voltage that may be continuously applied to the main terminals (anode, cathode) of an SCR. (Figure AN1008.1) An open-gate condition and gate resistance termination is designated for this rating. An increased reverse leakage can result due to a positive gate bias during the reverse voltage exposure time of the SCR. The repetitive peak reverse voltage rating relates to case temperatures up to the maximum rated junction temperature.

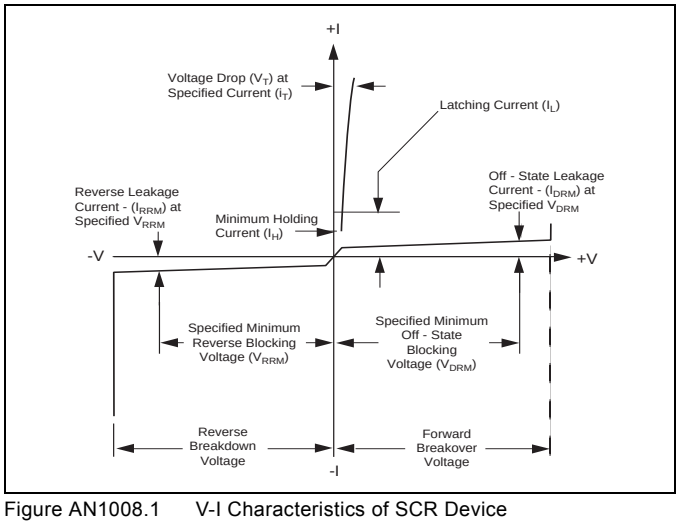


Figure AN1008.1 V-I Characteristics of SCR Device

V_{DRM}: Peak Repetitive Forward (Off-state) Voltage

SCR

The peak repetitive forward (off-state) voltage rating (Figure AN1008.1) refers to the maximum peak forward voltage which may be applied continuously to the main terminals (anode, cathode) of an SCR. This rating represents the maximum voltage the SCR should be required to block in the forward direction. The SCR may or may not go into conduction at voltages above the V_{DRM} rating. This rating is specified for an open-gate condition and gate resistance termination. A positive gate bias should be avoided since it will reduce the forward-voltage blocking capability. The peak repetitive forward (off-state) voltage rating applies for case temperatures up to the maximum rated junction temperature.

Triac

The peak repetitive off-state voltage rating should not be surpassed on a typical, non-transient, working basis. (Figure AN1008.2) V_{DRM} should not be exceeded even instantaneously. This rating applies for either positive or negative bias on main terminal 2 at the rated junction temperature. This voltage is less than the minimum breakover voltage so that breakover will not occur during operation. Leakage current is controlled at this voltage so that the temperature rise due to leakage power does not contribute significantly to the total temperature rise at rated current.

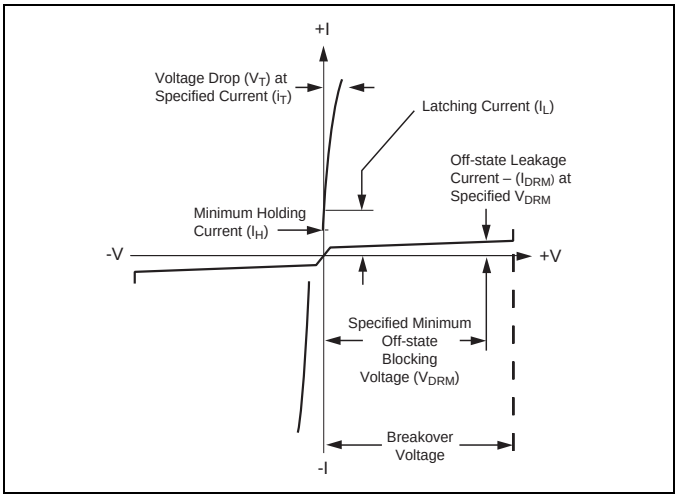


Figure AN1008.2 V-I Characteristics of Triac Device

I_T: Current Rating

SCR

For RMS and average currents, the restricting factor is usually confined so that the power dissipated during the on state and as a result of the junction-to-case thermal resistance will not produce a junction temperature in excess of the maximum junction temperature rating. Power dissipation is changed to RMS and average current ratings for a 60 Hz sine wave with a 180° conduction angle. The average current for conduction angles less than 180° is derated because of the higher RMS current connected with high peak currents. The DC current rating is higher than the average value for 180° conduction since no RMS component is present.

The dissipation for non-sinusoidal waveshapes can be determined in several ways. Graphically plotting instantaneous dissipation as a function of time is one method. The total maximum allowable power dissipation (P_D) may be determined using the following equation for temperature rise:

$$P_D = \frac{T_{J(MAX)} - T_C}{R_{\theta JC}}$$

where T_J(max) is the maximum rated junction temperature (at zero rated current), T_C is the actual operating case temperature, and $R_{\theta JC}$ is the published junction-to-case thermal resistance. Transient thermal resistance curves are required for short interval pulses.

Triac

The limiting factor for RMS current is determined by multiplying power dissipation by thermal resistance. The resulting current value will ensure an operating junction temperature within maximum value. For convenience, dissipation is converted to RMS current at a 360° conduction angle. The same RMS current can be used at a conduction angle of less than 360°. For information on non-sinusoidal waveshapes and a discussion of dissipation, refer to the preceding description of SCR current rating.

I_{TSM}: Peak Surge (Non-repetitive) On-state Current — SCR and Triac

The peak surge current is the maximum peak current that may be applied to the device for one full cycle of conduction without device degradation. The maximum peak current is usually specified as sinusoidal at 50 Hz or 60 Hz. This rating applies when the device is conducting rated current before the surge and, thus, with the junction temperature at rated values before the surge. The junction temperature will surpass the rated operating temperature during the surge, and the blocking capacity may be decreased until the device reverts to thermal equilibrium.

The surge-current curve in Figure AN1008.3 illustrates the peak current that may be applied as a function of surge duration. This surge curve is not intended to depict an exponential current decay as a function of applied overload. Instead, the peak current shown for a given number of cycles is the maximum peak surge permitted for that time period. The current must be derated so that the peak junction temperature during the surge overload does not exceed maximum rated junction temperature if blocking is to be retained after a surge.

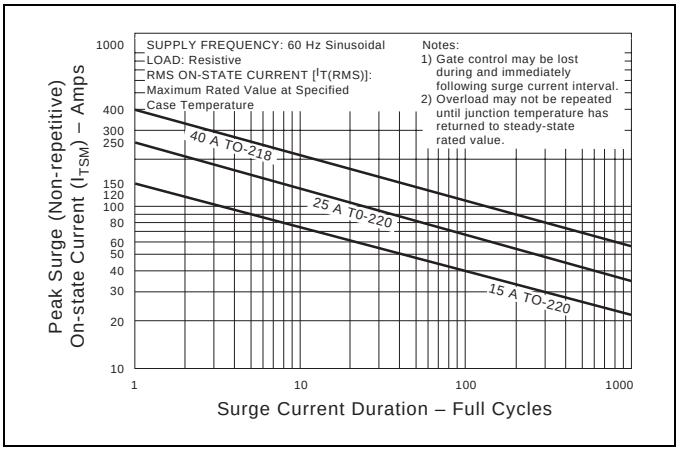


Figure AN1008.3 Peak Surge Current versus Surge Current Duration

I_{TM}: Peak Repetitive On-state Current — SCR and Triac

The I_{TM} rating specifies the maximum peak current that may be applied to the device during brief pulses. When the device operates under these circumstances, blocking capability is maintained. The minimum pulse duration and shape are defined and control the applied di/dt. The operating voltage, the duty factor, the case temperature, and the gate waveform are also defined. This rating must be followed when high repetitive peak currents are employed, such as in pulse modulators, capacitive-discharge circuits, and other applications where snubbers are required.

di/dt: Rate-of-change of On-state Current — SCR and Triac

The di/dt rating specifies the maximum rate-of-rise of current through a thyristor device during turn-on. The value of principal voltage prior to turn-on and the magnitude and rise time of the gate trigger waveform during turn-on are among the conditions under which the rating applies. If the rate-of-change of current (di/dt) exceeds this maximum value, or if turn-on with high di/dt during minimum gate drive occurs (such as dv/dt or overvoltage events), then localized heating may cause device degradation.

During the first few microseconds of initial turn-on, the effect of di/dt is more pronounced. The di/dt capability of the thyristor is greatly increased as soon as the total area of the pellet is in full conduction.

The di/dt effects that can occur as a result of voltage or transient turn-on (non-gated) is not related to this rating. The di/dt rating is specified for maximum junction temperature.

As shown in Figure AN1008.4, the di/dt of a surge current can be calculated by means of the following equation.

$$\frac{di}{dt} = \frac{\pi(I_{TM})}{t}$$

As an example, surge current of 400 A at 60 Hz has a di/dt of π400/8.3 or 151.4 A/ms.

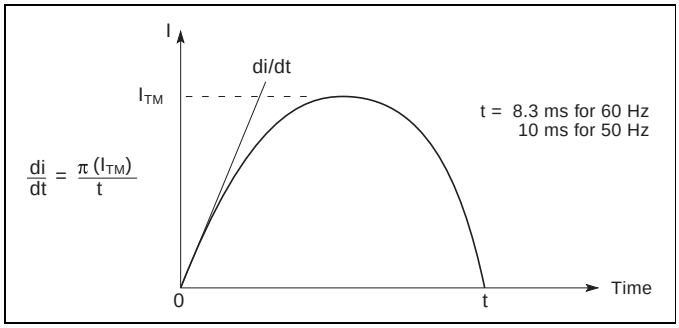


Figure AN1008.4 Relationship of Maximum Current Rating to Time

I^2t Rating — SCR and Triac

The I^2t rating gives an indication of the energy-absorbing capability of the thyristor device during surge-overload conditions. The rating is the product of the square of the RMS current $(I_{RMS})^2$ that flows through the device and the time during which the current is present and is expressed in A^2s. This rating is given for fuse selection purposes. It is important that the I^2t rating of the fuse is less than that of the thyristor device. Without proper fuse or current limit, overload or surge current will permanently damage the device due to excessive junction heating.

P_G: Gate Power Dissipation — SCR and Triac

Gate power dissipation ratings define both the peak power (P_{GM}) forward or reverse and the average power ($P_{G(AV)}$) that may be applied to the gate. Damage to the gate can occur if these ratings are not observed. The width of the applied gate pulses must be considered in calculating the voltage and current allowed since the peak power allowed is a function of time. The peak power that results from a given signal source relies on the gate characteristics of the specific unit. The average power resulting from high peak powers must not exceed the average-power rating.

T_S, T_J: Temperature Range — SCR and Triac

The maximum storage temperature (T_S) is greater than the maximum operating temperature (actually maximum junction temperature). Maximum storage temperature is restricted by material limits defined not so much by the silicon but by peripheral materials such as solders used on the chip/die and lead attachments as well as the encapsulating epoxy. The forward and off-state blocking capability of the device determines the maximum junction (T_J) temperature. Maximum blocking voltage and leakage current ratings are established at elevated temperatures near maximum junction temperature; therefore, operation in excess of these limits may result in unreliable operation of the thyristor.

Characteristics

V_{BO}: Instantaneous Breakover Voltage — SCR and Triac

Breakover voltage is the voltage at which a device turns on (switches to on state by voltage breakover). (Figure AN1008.1) This value applies for open-gate or gate-resistance termination. Positive gate bias lowers the breakover voltage. Breakover is temperature sensitive and will occur at a higher voltage if the junction temperature is kept below maximum T_J value. If SCRs and triacs are turned on as a result of an excess of breakover voltage, instantaneous power dissipations may be produced that can damage the chip or die.

I_{DRM}: Peak Repetitive Off-state (Blocking) Current

SCR

I_{DRM} is the maximum leakage current permitted through the SCR when the device is forward biased with rated positive voltage on the anode (DC or instantaneous) at rated junction temperature and with the gate open or gate resistance termination. A 1000 Ω resistor connected between gate and cathode is required on all sensitive SCRs. Leakage current decreases with decreasing junction temperatures. Effects of the off-state leakage currents on the load and other circuitry must be considered for each circuit application. Leakage currents can usually be ignored in applications that control high power.

Triac

The description of peak off-state (blocking/leakage) current for the triac is the same as for the SCR except that it applies with either positive or negative bias on main terminal 2. (Figure AN1008.2)

I_{RRM}: Peak Repetitive Reverse Current — SCR

This characteristic is essentially the same as the peak forward off-state (blocking/leakage) current except negative voltage is applied to the anode (reverse biased).

V_{TM}: Peak On-State Voltage — SCR and Triac

The instantaneous on-state voltage (forward drop) is the principal voltage at a specified instantaneous current and case temperature when the thyristor is in the conducting state. To prevent heating of the junction, this characteristic is measured with a short current pulse. The current pulse should be at least 100 µs duration to ensure the device is in full conduction. The forward-drop characteristic determines the on-state dissipation. See Figure AN1008.5, and refer to “IT: Current Rating” on page AN1008-2.

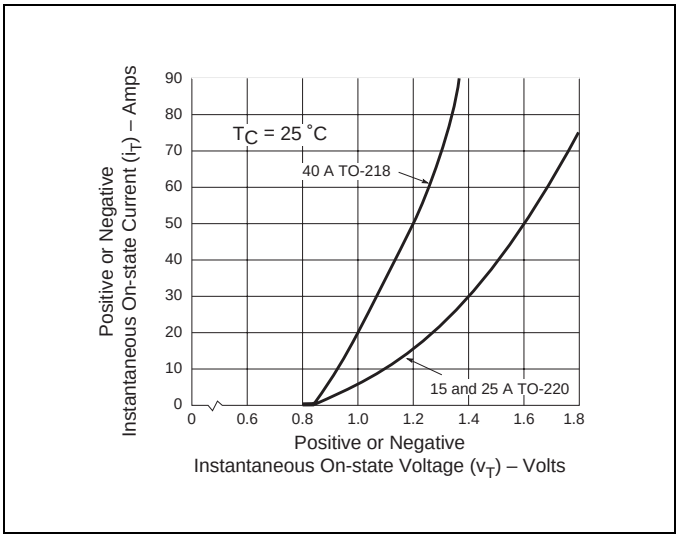


Figure AN1008.5 On-state Current versus On-state Voltage (Typical)

I_{GT}: DC Gate Trigger Current

SCR

I_{GT} is the minimum DC gate current required to cause the thyristor to switch from the non-conducting to the conducting state for a specified load voltage and current as well as case temperature. The characteristic curve illustrated in Figure AN1008.6 shows that trigger current is temperature dependent. The thyristor becomes less sensitive (requires more gate current) with decreasing junction temperatures. The gate current should be increased by a factor of two to five times the minimum threshold DC trigger current for best operation. Where fast turn-on is demanded and high di/dt is present or low temperatures are expected, the gate pulse may be 10 times the minimum I_{GT}, plus it must be fast-rising and of sufficient duration in order to properly turn on the thyristor.

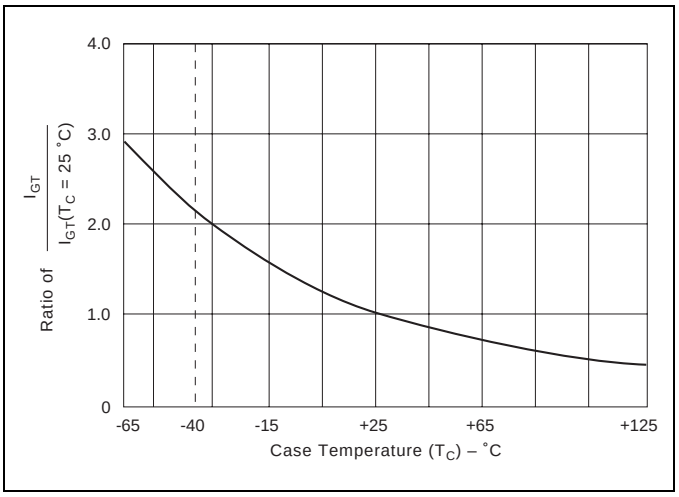


Figure AN1008.6 Normalized DC Gate Trigger Current for All Quadrants versus Case Temperature

Triac

The description for the SCR applies as well to the triac with the addition that the triac can be fired in four possible modes (Figure AN1008.7):

Quadrant I (main terminal 2 positive, gate positive)
Quadrant II (main terminal 2 positive, gate negative)
Quadrant III (main terminal 2 negative, gate negative)
Quadrant IV (main terminal 2 negative, gate positive)

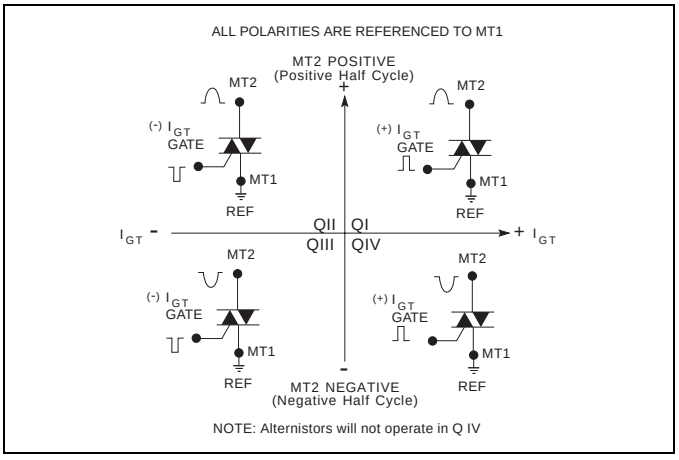


Figure AN1008.7 Definition of Operating Quadrants

V_{GT}: DC Gate Trigger Voltage

SCR

V_{GT} is the DC gate-cathode voltage that is present just prior to triggering when the gate current equals the DC trigger current. As shown in the characteristic curve in Figure AN1008.8, the gate trigger voltage is higher at lower temperatures. The gate-cathode voltage drop can be higher than the DC trigger level if the gate is driven by a current higher than the trigger current.

Triac

The difference in V_{GT} for the SCR and the triac is that the triac can be fired in four possible modes. The threshold trigger voltage can be slightly different, depending on which of the four operating modes is actually used.

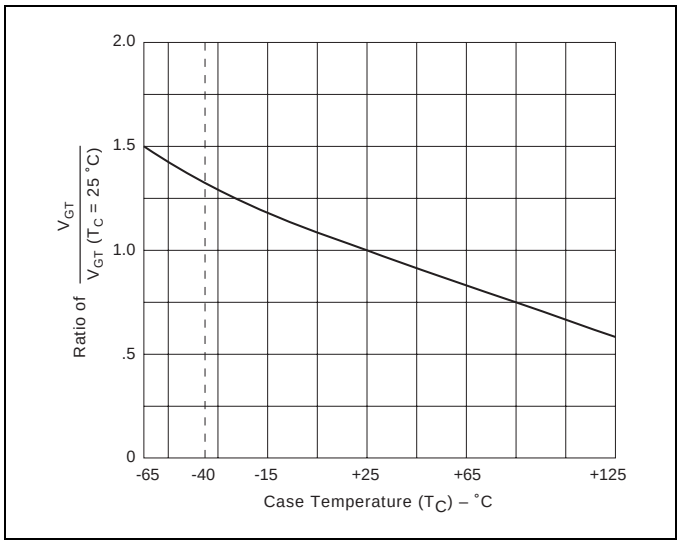


Figure AN1008.8 Normalized DC Gate Trigger Voltage for All Quadrants versus Case Temperature

I_L: Latching Current

SCR

Latching current is the DC anode current above which the gate signal can be withdrawn and the device stays on. It is related to, has the same temperature dependence as, and is somewhat greater than the DC gate trigger current. (Figure AN1008.1 and Figure AN1008.2) Latching current is at least equal to or much greater than the holding current, depending on the thyristor type.

Latching current is greater for fast-rise-time anode currents since not all of the chip/die is in conduction. It is this dynamic latching current that determines whether a device will stay on when the gate signal is replaced with very short gate pulses. The dynamic latching current varies with the magnitude of the gate drive current and pulse duration. In some circuits, the anode current may oscillate and drop back below the holding level or may even go negative; hence, the unit may turn off and not latch if the gate signal is removed too quickly.

Triac

The description of this characteristic for the triac is the same as for the SCR, with the addition that the triac can be latched on in four possible modes (quadrants). Also, the required latching is significantly different depending on which gating quadrants are used. Figure AN1008.9 illustrates typical latching current requirements for the four possible quadrants of operation.

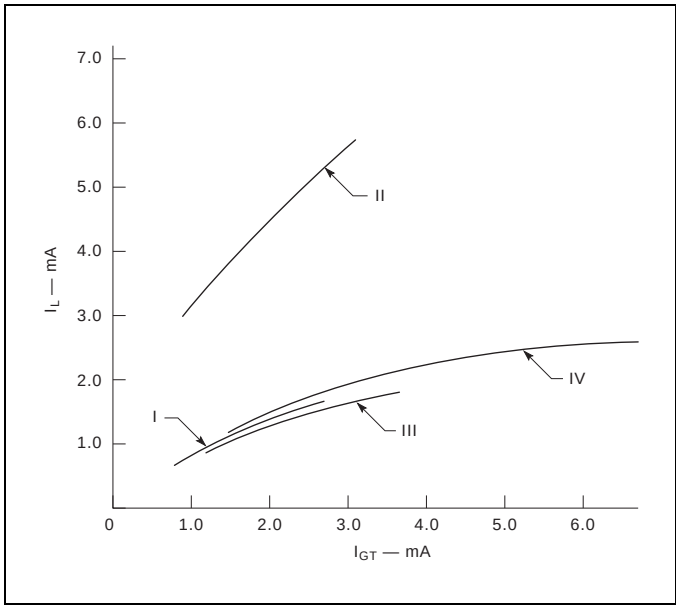


Figure AN1008.9 Typical Triac Latching (I_L) Requirements for Four Quadrants versus Gate Current (I_{GT})

I_H: Holding Current — SCR and Triac

The holding current is the DC principal on-state current below which the device will not stay in regeneration/on state after latching and gate signal is removed. This current is equal to or lower in value than the latching current (Figure AN1008.1 and Figure AN1008.2) and is related to and has the same temperature dependence as the DC gate trigger current shown in Figure AN1008.10. Both minimum and maximum holding current may be important. If the device is to stay in conduction at low-anode currents, the maximum holding current of a device for a given circuit must be considered. The minimum holding current of a device must be considered if the device is expected to turn off at a low DC anode current. Note that the low DC principal current condition is a DC turn-off mode, and that an initial on-state current (latching current) is required to ensure that the thyristor has been fully turned on prior to a holding current measurement.

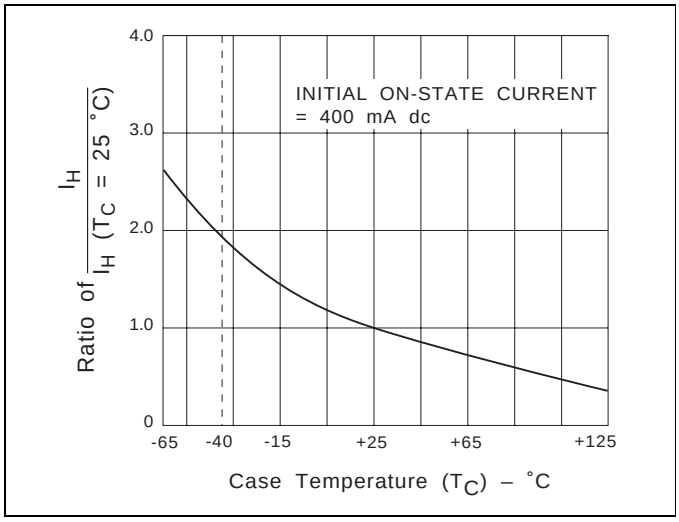


Figure AN1008.10 Normalized DC Holding Current versus Case Temperature

dv/dt, Static: Critical Rate-of-rise of Off-state Voltage — SCR and Triac

Static dv/dt is the minimum rate-of-rise of off-state voltage that a device will hold off, with gate open, without turning on. Figure AN1008.11 illustrates the exponential definition. This value will be reduced by a positive gate signal. This characteristic is temperature-dependent and is lowest at the maximum-rated junction temperature. Therefore, the characteristic is determined at rated junction temperature and at rated forward off-state voltage which is also a worst-case situation. Line or other transients which might be applied to the thyristor in the off state must be reduced, so that neither the rate-of-rise nor the peak voltage are above specifications if false firing is to be prevented. Turn-on as result of dv/dt is non-destructive as long as the follow current remains within current ratings of the device being used.

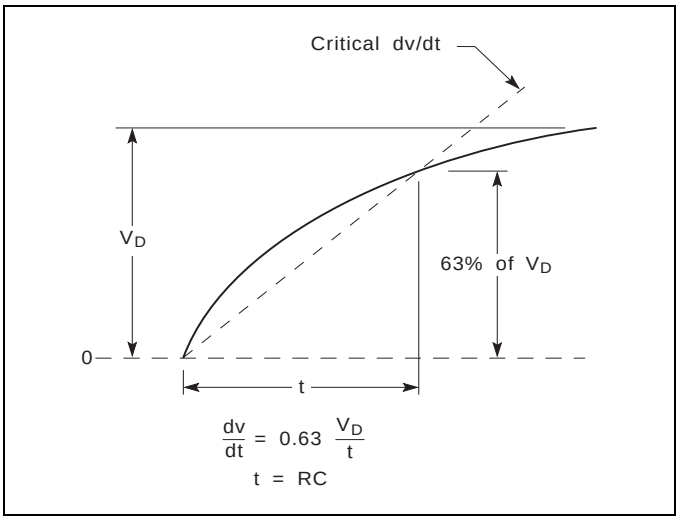


Figure AN1008.11 Exponential Rate-of-rise of Off-state Voltage Defining dv/dt

dv/dt, Commutating: Critical Rate-of-rise of Commutation Voltage — Triac

Commutating dv/dt is the rate-of-rise of voltage across the main terminals that a triac can support (block without switching back on) when commutating from the on state in one half cycle to the off state in the opposite half cycle. This parameter is specified at maximum rated case temperature (equal to T_J) since it is temperature-dependent. It is also dependent on current (commutating di/dt) and peak reapplied voltage (line voltage) and is specified at rated current and voltage. All devices are guaranteed to commutate rated current with a resistive load at 50 Hz to 60 Hz. Commutation of rated current is not guaranteed at higher frequencies, and no direct relationship can be made with regard to current/temperature derating for higher-frequency operation. With inductive loading, when the voltage is out of phase with the load current, a voltage stress (dv/dt) occurs across the main terminals of the triac during the zero-current crossing. (Figure AN1008.12) A snubber (series RC across the triac) should be used with inductive loads to decrease the applied dv/dt to an amount below the minimum value which the triac can be guaranteed to commutate off each half cycle.

Commutating dv/dt is specified for a half sinewave current at 60 Hz which fixes the di/dt of the commutating current. The commutating di/dt for 50 Hz is approximately 20% lower while I_{RMS} rating remains the same. (Figure AN1008.4)

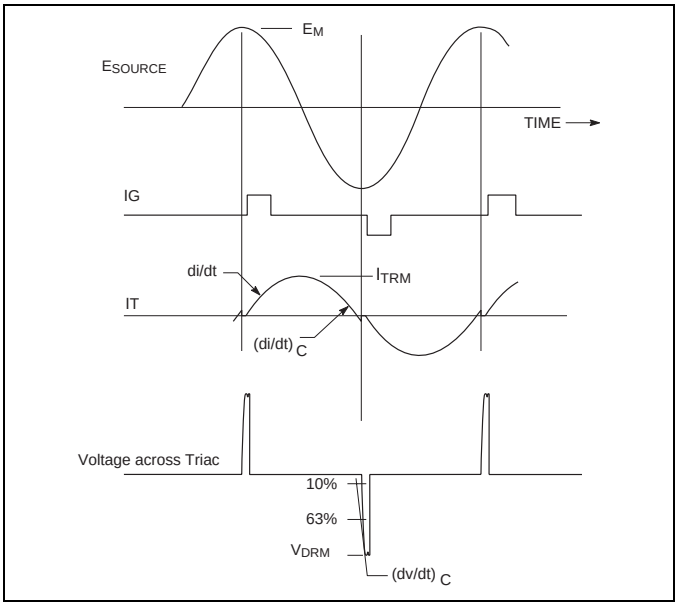


Figure AN1008.12 Waveshapes of Commutating dv/dt and Associated Conditions

t_{gt}: Gate-controlled Turn-on Time — SCR and Triac

The t_{gt} is the time interval between the application of a gate pulse and the on-state current reaching 90% of its steady-state value. (Figure AN1008.13) As would be expected, turn-on time is a function of gate drive. Shorter turn-on times occur for increased gate drives. This turn-on time is actually only valid for resistive loading. For example, inductive loading would restrict the rate-of-rise of anode current. For this reason, this parameter does not indicate the time that must be allowed for the device to stay on if the gate signal is removed. (Refer to the description of "IL: Latching Current" on page AN1008-4.) However, if the load was resistive and equal to the rated load current value, the device definitely would be operating at a current above the dynamic latching current in the turn-on time interval since current through the device is at 90% of its peak value during this interval.

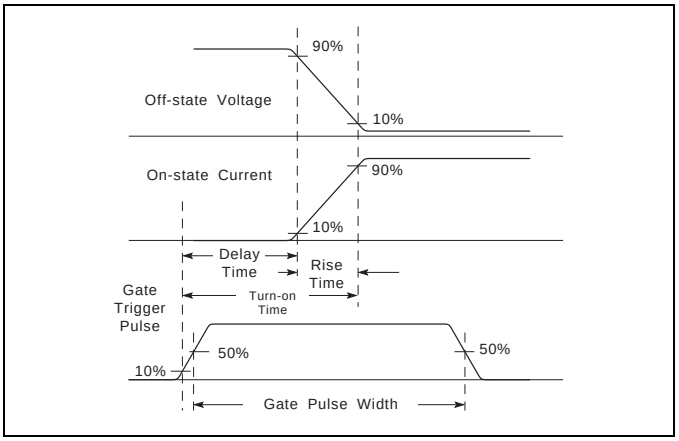


Figure AN1008.13 Waveshapes for Turn-on Time and Associated Conditions

t_q: Circuit-commutated Turn-off Time — SCR

The circuit-commutated turn-off time of the device is the time during which the circuit provides reverse bias to the device (negative anode) to commutate it off. The turn-off time occurs between the time when the anode current goes negative and when the anode positive voltage may be reapplied. (Figure AN1008.14) Turn-off time is a function of many parameters and very dependent on temperature and gate bias during the turn-off interval. Turn-off time is lengthened for higher temperature so a high junction temperature is specified. The gate is open during the turn-off interval. Positive bias on the gate will lengthen the turn-off time; negative bias on the gate will shorten it.

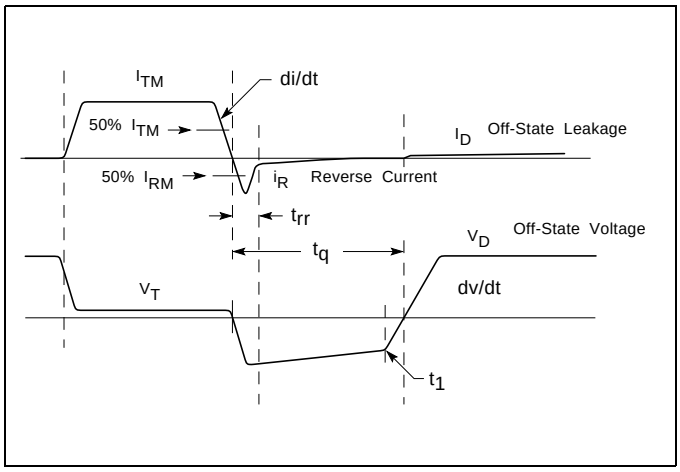


Figure AN1008.14 Waveshapes of t_q Rating Test and Associated Conditions

$R_{\theta JC}$, $R_{\theta JA}$: Thermal Resistance (Junction-to-case, Junction-to-ambient) — SCR and Triac

The thermal-resistance characteristic defines the steady-state temperature difference between two points at a given rate of heat-energy transfer (dissipation) between the points. The thermal-resistance system is an analog to an electrical circuit where thermal resistance is equivalent to electrical resistance, temperature difference is equivalent to voltage difference, and rate of heat-energy transfer (dissipation) is equivalent to current. Dissipation is represented by a constant current generator since generated heat must flow (steady-state) no matter what the resistance in its path. Junction-to-case thermal resistance establishes the maximum case temperature at maximum rated steady-state current. The case temperature must be held to the maximum at maximum ambient temperature when the device is operating at rated current. Junction-to-ambient thermal resistance is established at a lower steady-state current, where the device is in free air with only the external heat sinking offered by the device package itself. For $R_{\theta JA}$, power dissipation is limited by what the device package can dissipate in free air without any additional heat sink:

$$R\theta JC = \frac{T_J - T_C}{P_{(AV)}}$$

$$R\theta JA = \frac{T_J - T_A}{P_{(AV)}}$$

AN1009

Miscellaneous Design Tips and Facts

Introduction

This application note presents design tips and facts on the following topics:

- Relationship of I_{AV}, I_{RMS}, and I_{PK}
- dv/dt Definitions
- Examples of gate terminations
- Curves for Average Current at Various Conduction Angles
- Double-exponential Impulse Waveform
- Failure Modes of Thyristor
- Characteristics Formulas for Phase Control Circuits

Relationship of I_{AV}, I_{RMS}, and I_{PK}

Since a single rectifier or SCR passes current in one direction only, it conducts for only half of each cycle of an AC sinewave. The average current (I_{AV}) then becomes half of the value determined for full-cycle conduction, and the RMS current (I_{RMS}) is equal to the square root of half the mean-square value for full-cycle conduction or half the peak current (I_{PK}). In terms of half-cycle sinewave conduction (as in a single-phase half-wave circuit), the relationships of the rectifier currents can be shown as follows:

$I_{PK} = \pi \ I_{AV} = 3.14 \ I_{AV}$
$I_{AV} = (1/\pi) \ I_{PK} = 0.32 \ I_{PK}$
$I_{PK} = 2 \ I_{RMS}$
$I_{RMS} = 0.5 \ I_{PK}$
$I_{AV} = (2/\pi) \ I_{RMS} = 0.64 \ I_{RMS}$
$I_{RMS} = (\pi/2) \ I_{AV} = 1.57 \ I_{AV}$

When two identically rated SCRs are connected inverse parallel for full-wave operation, as shown in Figure AN1009.1, they can handle 1.41 times the RMS current rating of either single SCR. Therefore, the RMS value of two half sinewave current pulses in one cycle is $\sqrt{2}$ times the RMS value of one such pulse per cycle.

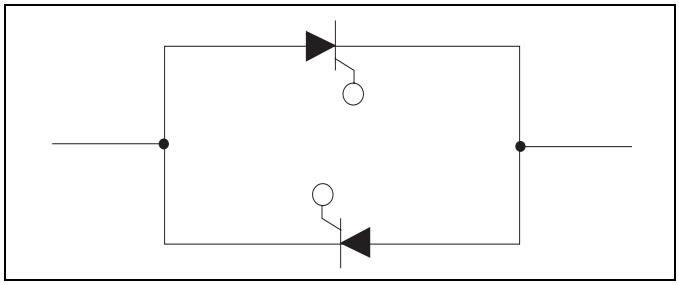


Figure AN1009.1 SCR Anti-parallel Circuit

dv/dt Definitions

The rate-of-rise of voltage (dv/dt) of an **exponential waveform** is 63% of peak voltage (excluding any overshoots) divided by the time at 63% minus 10% peak voltage. (Figure AN1009.2)

$$\text{Exponential dv/dt} = 0.63 \bullet [V_{PK}] = (t_2 - t_1)$$

$$\text{Resistor Capacitor circuit } t = RC = (t_2 - t_1)$$

$$\text{Resistor Capacitor circuit } 4 \bullet RC = (t_3 - t_2)$$

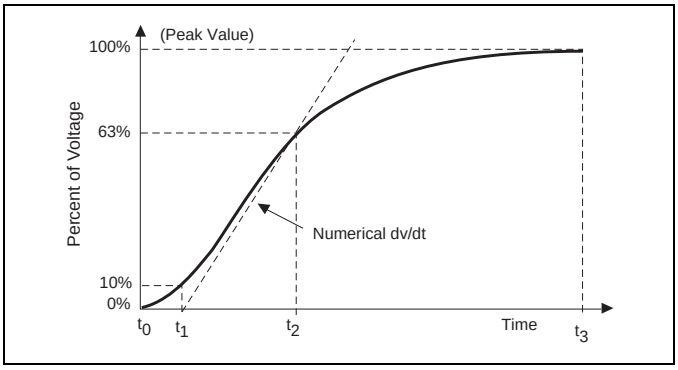


Figure AN1009.2 Exponential dv/dt Waveform

The rate-of-rise of voltage (dv/dt) of a **linear waveform** is 80% of peak voltage (excluding any overshoots) divided by the time at 90% minus 10% peak voltage. (Figure AN1009.3)

$$\text{Linear dv/dt} = 0.8 \bullet [V_{PK}] = (t_2 - t_1)$$

$$\text{Linear dv/dt} = [0.9 \bullet V_{PK} - 0.1 \bullet V_{PK}] = (t_2 - t_1)$$

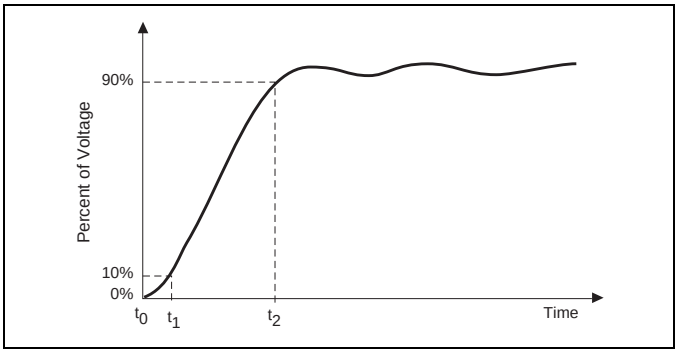
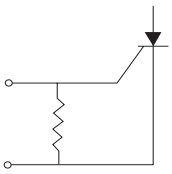


Figure AN1009.3 Linear dv/dt Waveform

Examples of Gate Terminations



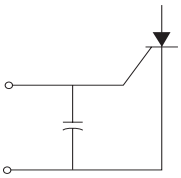
Primary Purpose

(1) Increase dv/dt capability

(2) Keep gate clamped to ensure V_{DRM} capability

(3) Lower t_q time

Related Effect — Raises the device latching and holding current



Primary Purpose

(1) Increase dv/dt capability

(2) Remove high frequency noise

Related Effects

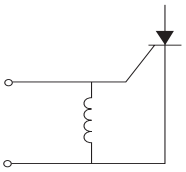
(1) Increases delay time

(2) Increases turn-on interval

(3) Lowers gate signal rise time

(4) Lowers di/dt capability

(5) Increases t_q time



Primary Purpose

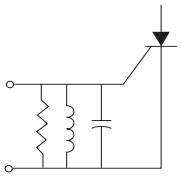
(1) Decrease DC gate sensitivity

(2) Decrease t_q time

Related Effects

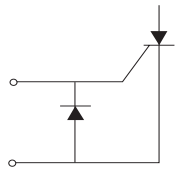
(1) Negative gate current increases holding current and causes gate area to drop out of conduction

(2) In pulse gating gate signal tail may cause device to drop out of conduction



Primary Purpose — Select frequency

Related Effects — Unless circuit is "damped," positive and negative gate current may inhibit conduction or bring about sporadic anode current



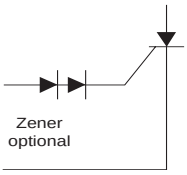
Primary Purpose

(1) Supply reverse bias in off period

(2) Protect gate and gate supply for reverse transients

(3) Lower t_q time

Related Effects — Isolates the gate if high impedance signal source is used without sustained diode current in the negative cycle

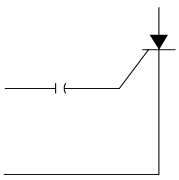


Primary Purpose — Decrease threshold sensitivity

Related Effects

(1) Affects gate signal rise time and di/dt rating

(2) Isolates the gate



Primary Purpose — Isolate gate circuit DC component

Related Effects — In narrow gate pulses and low impedance sources, I_{gt} followed by reverse gate signals which may inhibit conduction

Curves for Average Current at Various Conduction Angles

SCR maximum average current curves for various conduction angles can be established using the factors for maximum average current at conduction angle of:

30° = 0.40 x Avg 180°
60° = 0.56 x Avg 180°
90° = 0.70 x Avg 180°
120° = 0.84 x Avg 180°

The reason for different ratings is that the average current for conduction angles less than 180° is derated because of the higher RMS current connected with high peak currents.

Note that maximum allowable case temperature (T_C) remains the same for each conduction angle curve but is established from average current rating at 180° conduction as given in the data sheet for any particular device type. The maximum T_C curve is then derated down to the maximum junction (T_J). The curves illustrated in Figure AN1009.4 are derated to 125 °C since the maximum T_J for the non-sensitive SCR series is 125 °C.

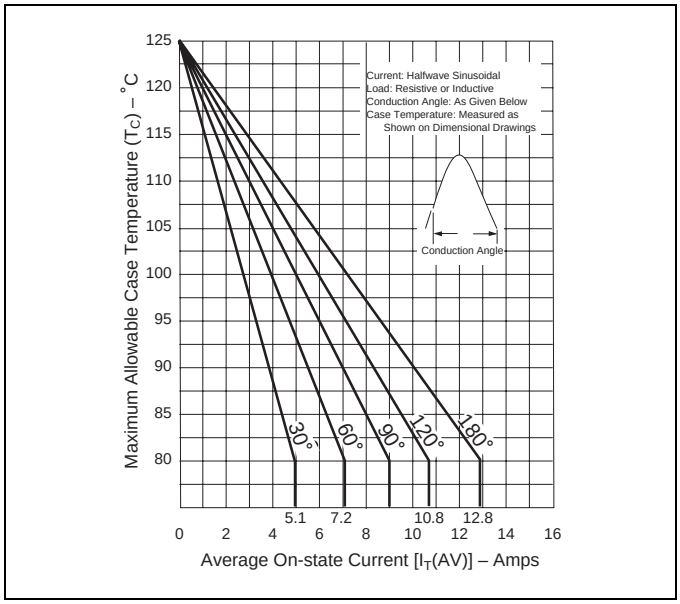


Figure AN1009.4 Typical Curves for Average On-state Current at Various Conduction Angles versus T_C for a SXX20L SCR

Double-exponential Impulse Waveform

A double-exponential impulse waveform or waveshape of current or voltage is designated by a combination of two numbers (t_r/t_d or t_r x t_d µs). The first number is an exponential rise time (t_r) or wave front and the second number is an exponential decay time (t_d) or wave tail. The rise time (t_r) is the maximum rise time permitted. The decay time (t_d) is the minimum time permitted. Both the t_r and the t_d are in the same units of time, typically microseconds, designated at the end of the waveform description as defined by ANSI/IEEE C62.1-1989.

The rise time (t_r) of a current waveform is 1.25 times the time for the current to increase from 10% to 90% of peak value. See Figure AN1009.5.

t_r = Rise Time = 1.25 • [t_c – t_a]
t_r = 1.25 • [$t(0.9\ I_{PK})$ – $t(0.1\ I_{PK})$] = T_1 – T_0

The rise time (t_r) of a voltage waveform is 1.67 times the time for the voltage to increase from 30% to 90% of peak value. (Figure AN1009.5)

t_r = Rise Time = 1.67 • [t_c – t_b]
t_r = 1.67 • [$t(0.9\ V_{PK})$ – $t(0.3\ V_{PK})$] = T_1 – T_0

The decay time (t_d) of a waveform is the time from virtual zero (10% of peak for current or 30% of peak for voltage) to the time at which one-half (50%) of the peak value is reached on the wave tail. (Figure AN1009.5)

Current Waveform t_d = Decay Time
= [$t(0.5\ I_{PK})$ – $t(0.1\ I_{PK})$] = T_2 – T_0

Voltage Waveform t_d = Decay Time
= [$t(0.5\ V_{PK})$ – $t(0.3\ V_{PK})$] = T_2 – T_0

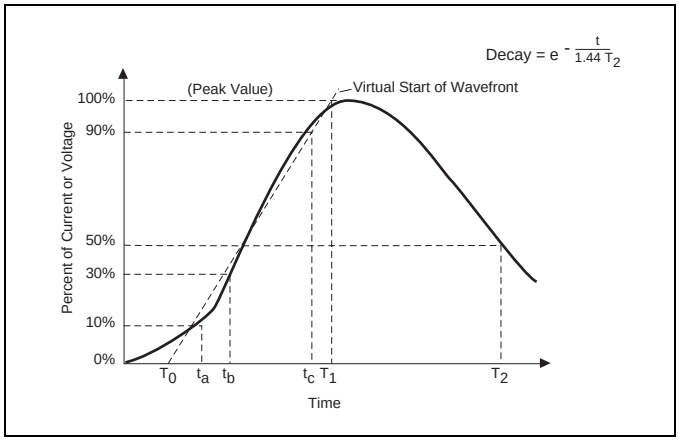


Figure AN1009.5 Double-exponential Impulse Waveform

Failure Modes of Thyristor

Thyristor failures may be broadly classified as either degrading or catastrophic. A degrading type of failure is defined as a change in some characteristic which may or may not cause a catastrophic failure, but could show up as a latent failure. Catastrophic failure is when a device exhibits a sudden change in characteristic that renders it inoperable. To minimize degrading and catastrophic failures, devices must be operated within maximum ratings at all times.

Degradation Failures

A significant change of on-state, gate, or switching characteristics is quite rare. The most vulnerable characteristic is blocking voltage. This type of degradation increases with rising operating voltage and temperature levels.

Catastrophic Failures

A catastrophic failure can occur whenever the thyristor is operated beyond its published ratings. The most common failure mode is an electrical short between the main terminals, although a triac can fail in a half-wave condition. It is possible, but not probable, that the resulting short-circuit current could melt the internal parts of the device which could result in an open circuit.

Failure Causes

Most thyristor failures occur due to exceeding the maximum operating ratings of the device. Overvoltage or overcurrent operations are the most probable cause for failure. Overvoltage failures may be due to excessive voltage transients or may also occur if inadequate cooling allows the operating temperature to rise above the maximum allowable junction temperature. Overcurrent failures are generally caused by improper fusing or circuit protection, surge current from load initiation, load abuse, or load failure. Another common cause of device failure is incorrect handling procedures used in the manufacturing process. Mechanical damage in the form of excessive mounting torque and/or force applied to the terminals or leads can transmit stresses to the internal thyristor chip and cause cracks in the chip which may not show up until the device is thermally cycled.

Prevention of Failures

Careful selection of the correct device for the application's operating parameters and environment will go a long way toward extending the operating life of the thyristor. Good design practice should also limit the maximum current through the main terminals to 75% of the device rating. Correct mounting and forming of the leads also help ensure against infant mortality and latent failures. The two best ways to ensure long life of a thyristor is by proper heat sink methods and correct voltage rating selection for worst case conditions. Overheating, overvoltage, and surge currents are the main killers of semiconductors.

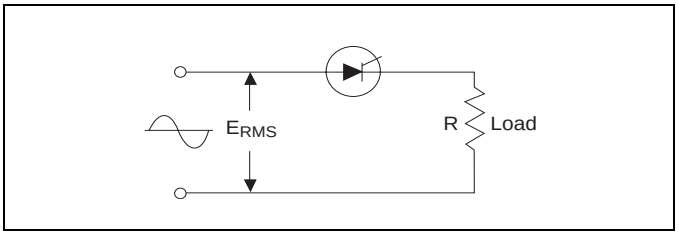
Most Common Thyristor Failure Mode

When a thyristor is electrically or physically abused and fails either by degradation or a catastrophic means, it will short (full-wave or half-wave) as its normal failure mode. Rarely does it fail open circuit. The circuit designer should add line breaks, fuses, overtemperature interrupters or whatever is necessary to protect the end user and property if a shorted or partially shorted thyristor offers a safety hazard.

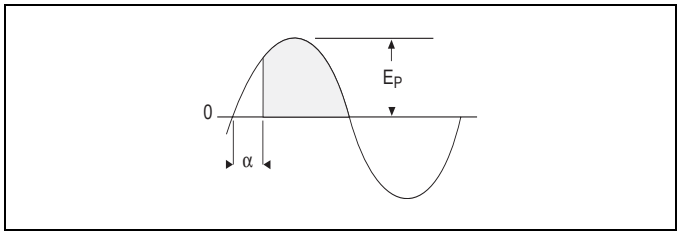
Characteristics Formulas for Phase Control Circuits

Circuit Name	Max Thyristor Voltage	PRV SCR	Max. Load Voltage E_d=Avg. E_a=RMS	Load Voltage with Delayed Firing	Max. Average Thyristor or Rectifier Current	
					Avg. Amps	Cond. Period
Half-wave Resistive Load	1.4 E_{RMS}	E_P	$E_d = \frac{E_P}{\pi}$ $E_a = \frac{E_P}{2}$	$E_d = \frac{E_P}{2\pi}(1+\cos\alpha)$ $E_a = \frac{E_P}{2\sqrt{\pi}}\sqrt{\left(\pi-\alpha+\frac{1}{2}\sin 2\alpha\right)}$	$\frac{E_P}{\pi R}$	180
Full-wave Bridge	1.4 E_{RMS}	E_P	$E_d = \frac{2E_P}{\pi}$	$E_d = \frac{E_P}{2\sqrt{\pi}}(1+\cos\alpha)$	$\frac{E_P}{\pi R}$	180
Full-wave AC Switch Resistive Load	1.4 E_{RMS}	E_P	$E_a = \frac{E_P}{1.4}$	$E_a = \frac{E_P}{\sqrt{2\pi}}\sqrt{\left(\pi-\alpha+\frac{1}{2}\sin 2\alpha\right)}$	$\frac{E_P}{\pi R}$	180

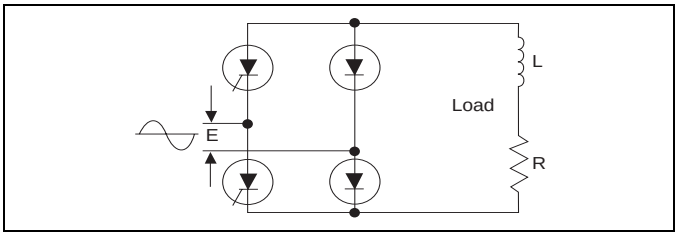
NOTE: Angle alpha (α) is in radians.



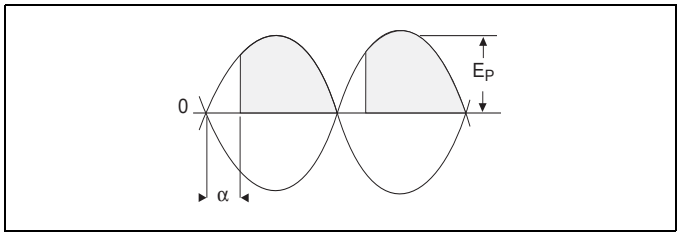
Half-wave Resistive Load – Schematic



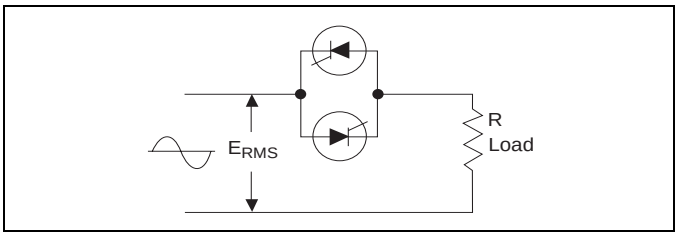
Half-wave Resistive Load – Waveform



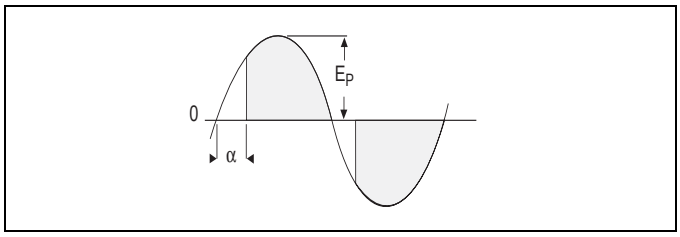
Full-wave Bridge – Schematic



Full-wave Bridge – Waveform



Full-wave AC Switch Resistive Load – Schematic



Full-wave AC Switch Resistive Load – Waveform

AN1010

Thyristors for Ignition of Fluorescent Lamps

Introduction

One of the many applications for Teccor thyristors is in fluorescent lighting. Standard conventional and circular fluorescent lamps with filaments can be ignited easily and much more quickly by using thyristors instead of the mechanical starter switch, and solid state thyristors are more reliable. Thyristors produce a pure solid state igniting circuit with no mechanical parts in the fluorescent lamp fixture. Also, because the lamp ignites much faster, the life of the fluorescent lamp can be increased since the filaments are activated for less time during the ignition. The thyristor ignition eliminates any audible noise or flashing off and on which most mechanical starters possess.

Standard Fluorescent Circuit

The standard starter assembly is a glow switch mechanism with option small capacitor in parallel. (Figure AN1010.1)

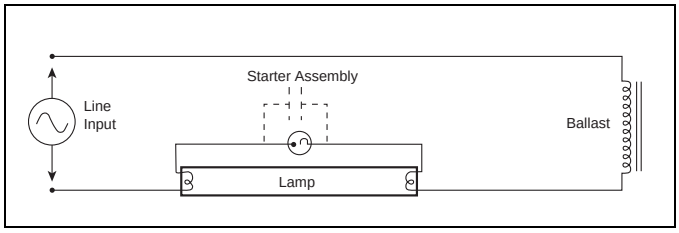


Figure AN1010.1 Typical Standard Fluorescent Circuit

The glow switch is made in a small glass bulb containing neon or argon gas. Inside the bulb is a U-shaped bimetallic strip and a fixed post. When the line input current is applied, the voltage between the bimetallic strip and the fixed post is high enough to ionize and produce a glow similar to a standard neon lamp. The heat from the ionization causes the bimetallic strip to move and make contact to the fixed post. At this time the ionization ceases and current can flow through and pre-heat the filaments of the fluorescent lamp.

Since ionization (glowing) has ceased, the bimetallic strip begins to cool down and in a few seconds opens to start ionization (glowing) again. The instant the bimetallic ceases to make contact (opens), an inductive kick from the ballast produces some high voltage spikes 400 V to 600 V, which can ignite (strike) the fluorescent lamp. If the lamp fails to ignite or start, the glow switch mechanically repeats its igniting cycle over and over until the lamp ignites, usually within a few seconds.

In this concept the ballast (inductor) is able to produce high voltage spikes using a mechanical switch opening and closing, which is fairly slow.

Since thyristors (solid state switches) do not mechanically open and close, the conventional fluorescent lighting circuit concept must be changed in order to use thyristors. In order to ignite (strike) a fluorescent lamp, a high voltage spike must be produced. The spike needs to be several hundred volts to quickly initiate ionization in the fluorescent lamp. A series ballast can only produce high voltage if a mechanical switch is used in conjunction with it. Therefore, with a thyristor, a standard series ballast (inductor) is only useful as a current limiter.

Methods for Producing High Voltage

The circuits illustrated in Figure AN1010.2 through Figure AN1010.5 show various methods for producing high voltage to ignite fluorescent lamps using thyristors (solid state switches).

Note: Due to many considerations in designing a fluorescent fixture, the illustrated circuits are not necessarily the optimum design.

One 120 V ac circuit consists of triac and diac thyristors with a capacitor to ignite the fluorescent lamp. (Figure AN1010.2)

This circuit allows the 5 µF ac capacitor to be charged and added to the peak line voltage, developing close to 300 V peak or 600 V peak to peak. This is accomplished by using a triac and diac phase control network set to fire near the 90° point of the input line. A capacitor-charging network is added to ensure that the capacitor is charged immediately, letting tolerances of components or temperature changes in the triac and diac circuit to be less critical. By setting the triac and diac phase control to fire at near the 90° point of the sinewave, maximum line voltages appear across the lamp for ignition. As the triac turns on during each half cycle, the filaments are pre-heated and in less than a second the lamp is lit. Once the lamp is lit the voltage is clamped to approximately 60 V peak across the 15 W to 20 W lamp, and the triac and diac circuit no longer functions until the lamp is required to be ignited again.

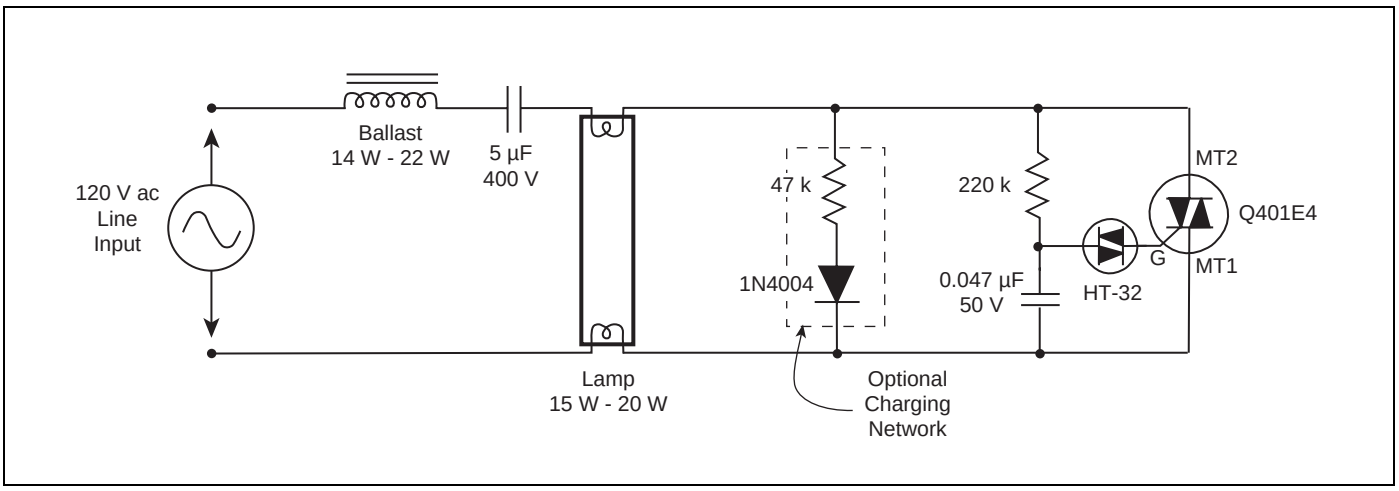


Figure AN1010.2 120 V ac Triac/Diac Circuit

Figure AN1010.3 illustrates a circuit using a sidac (a simpler thyristor) phase control network to ignite a 120 V ac fluorescent lamp. As in the triac/diac circuit, the 5 µF ac capacitor is charged and added to the peak line voltage, developing greater than 200 V peak or 400 V peak to peak. Since the sidac is a voltage breakover (V_{BO}) activated device with no gate, a charging network is essential in this circuit to charge the capacitor above the peak of the line in order to break over (turn on) the sidac with a V_{BO} of 220 V to 250 V.

As the sidac turns on each half cycle, the filaments are preheated and in less than 1.5 seconds the lamp is lit. Once the lamp is lit, the voltage across it clamps to approximately 60 V peak (for a 15 W to 20 W lamp), and the sidac ceases to function until the lamp is required to be ignited again.

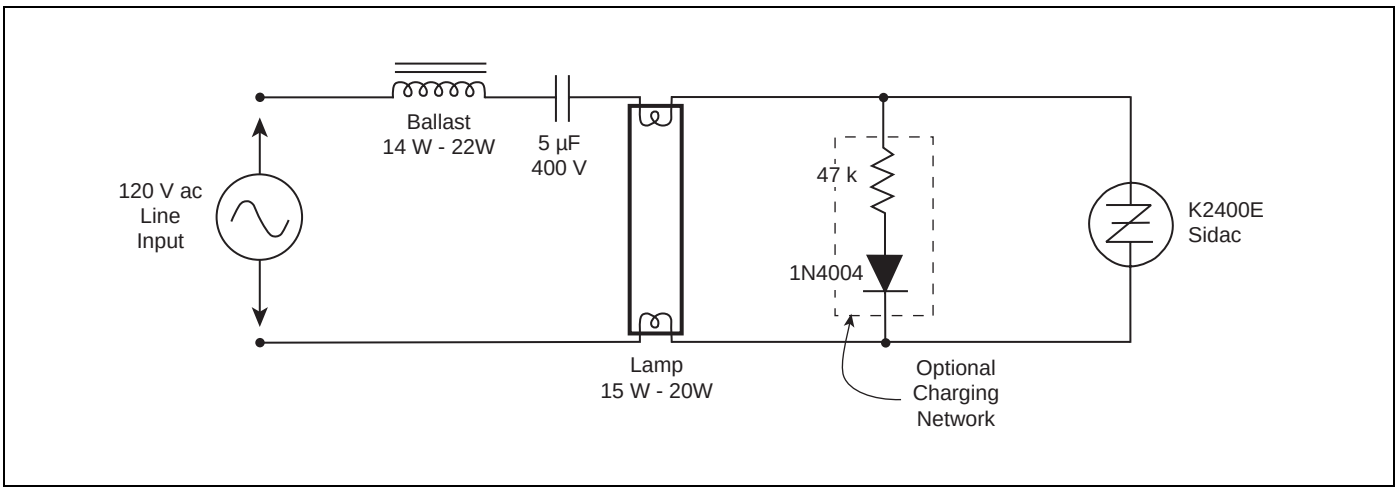


Figure AN1010.3 120 V ac Sidac Circuit

The circuits illustrated in Figure AN1010.2 and Figure AN1010.3 use 15 W to 20 W lamps. The same basic circuits can be applied to higher wattage lamps. However, with higher wattage lamps the voltage developed to fire (light) the lamp will need to be somewhat higher. For instance, a 40 W lamp is critical on line input voltage to ignite, and after it is lit the voltage across the lamp will clamp to approximately 130 V peak. For a given type of lamp, the current must be limited to constant current regardless of the wattage of the lamp.

Figure AN1010.4 shows a circuit for igniting a fluorescent lamp with 240 V line voltage input using triac and diac networks.

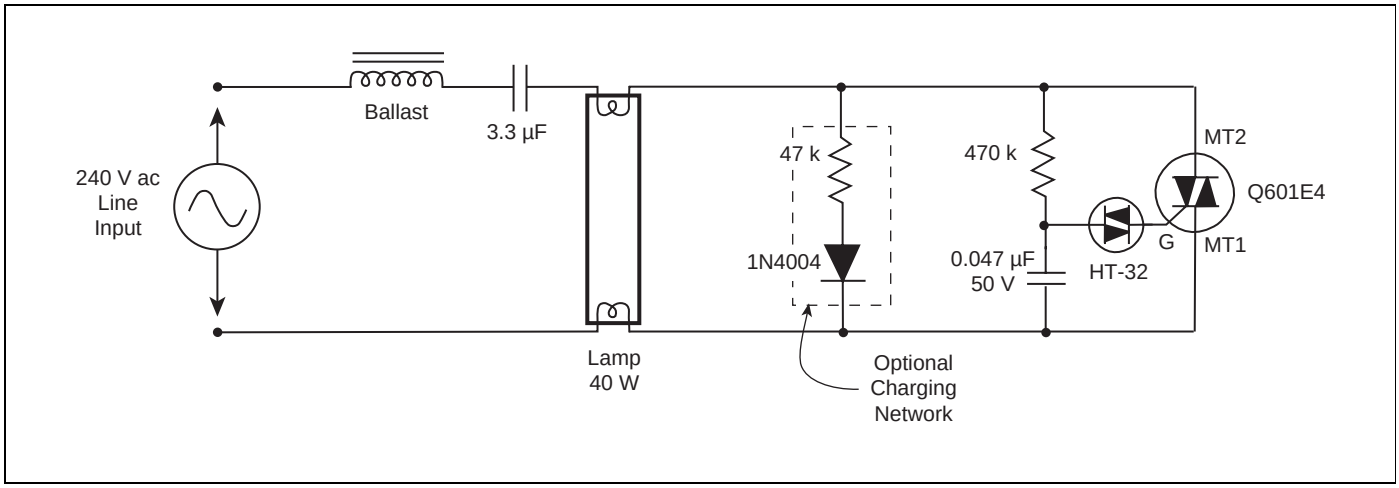


Figure AN1010.4 240 V ac Triac/Diac Circuit

Figure AN1010.5 illustrates a circuit using a sidac phase control network to ignite a 240 V ac fluorescent lamp. This circuit works basically the same as the 120 V circuit shown in Figure AN1010.3, except that component values are changed to compensate for higher voltage. The one major change is that two K2400E devices in series are used to accomplish high firing voltage for a fluorescent lamp.

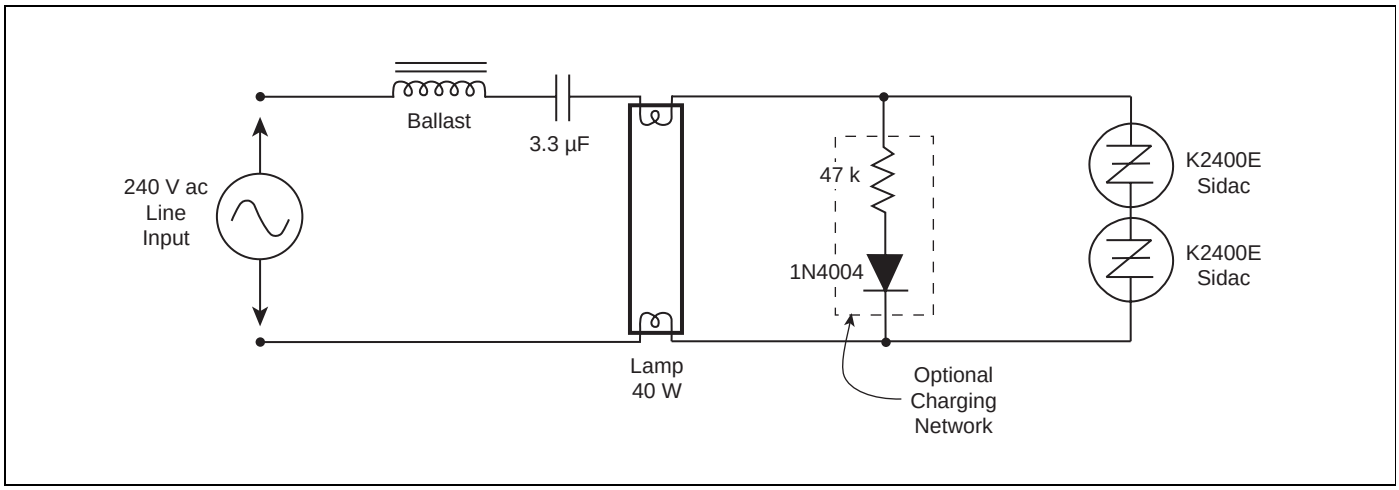


Figure AN1010.5 240 V ac Sidac Circuit

Notes